

Cottonwood Schematics

Skylake-U

2015-07-08

REV : A00

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DY : None Installed

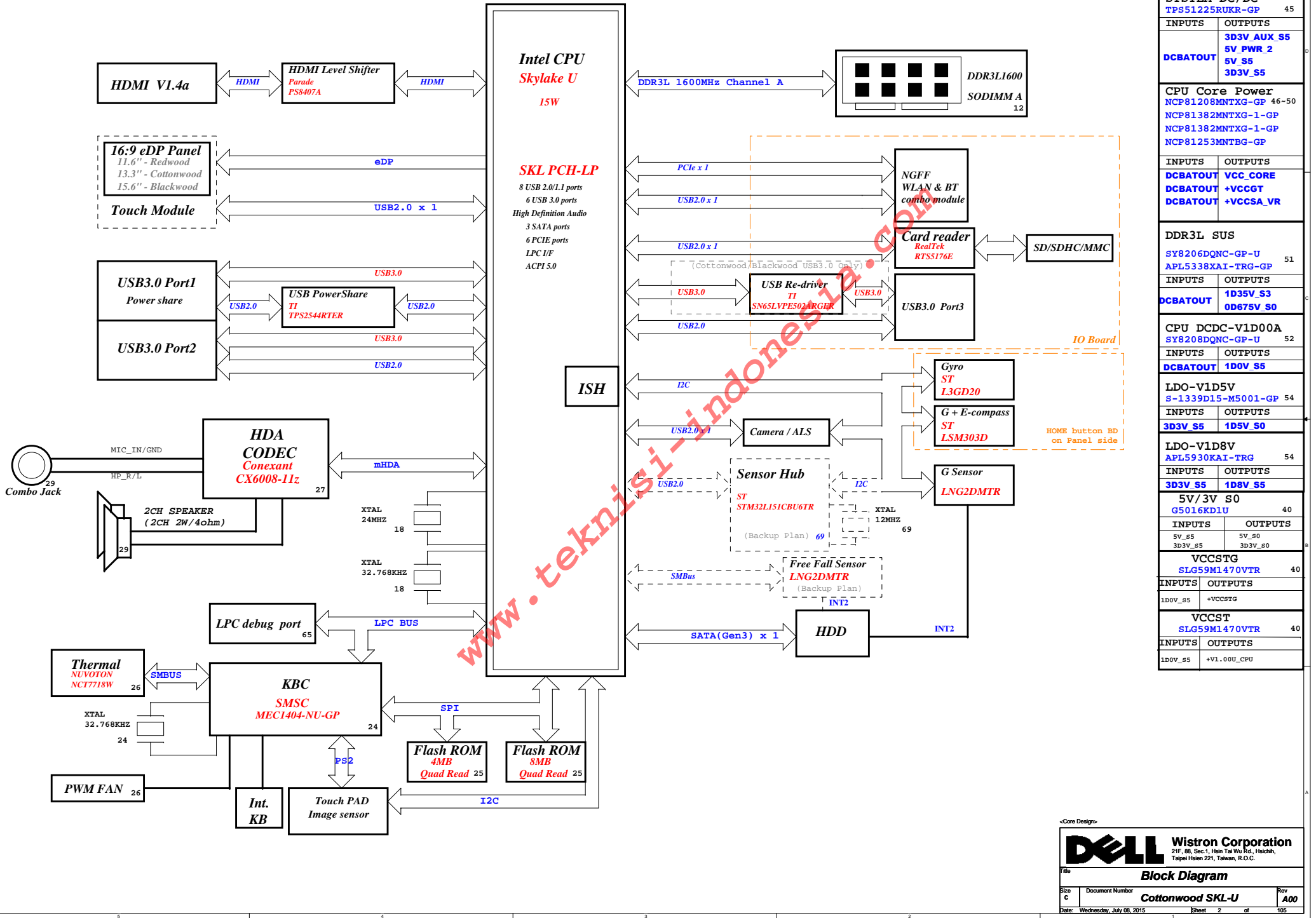
UMA: UMA only installed

OPS: DISCRTE OPTIMUS installed

<Variant Name>		
DELL Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
Cover Page		
Size A3	Document Number Cottonwood SKL-U	Rev A00
Date: Thursday, July 09, 2015	Sheet 1	of 105

Project code: 4PD05M010001
PCB P/N: 14275
Revision: A00

Cottonwood SKL-U Block Diagram

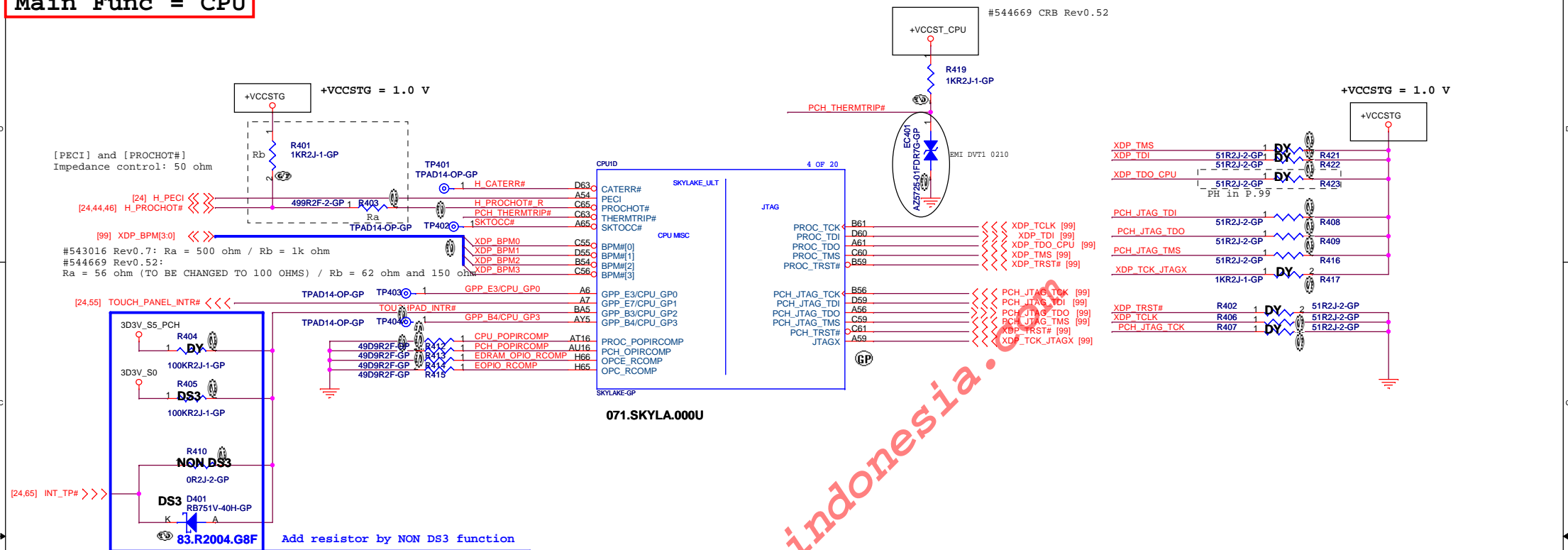


Main Func = CPU

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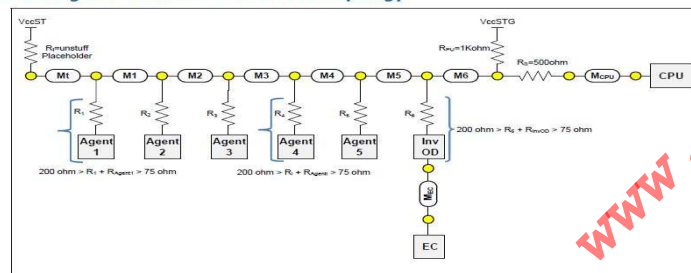
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Main Func = CPU



(#543016) PROCHOT# Routing Guidelines

Figure 10-1. Routing Illustration for PROCHOT# Topology



```

M1,2,3,4,5: <3 inches
M6: 1-11 inches
MCPU: 0.3-1.5 inches
Mt <0.3 mils
Main route(M1+M2+M3+M4+M5+M6+MCPU): 1-12 inches

```

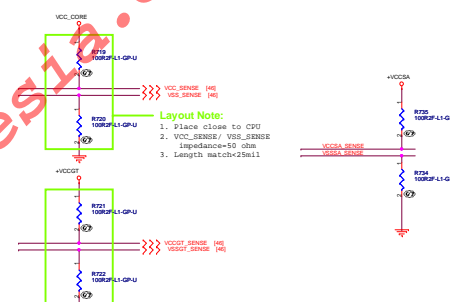
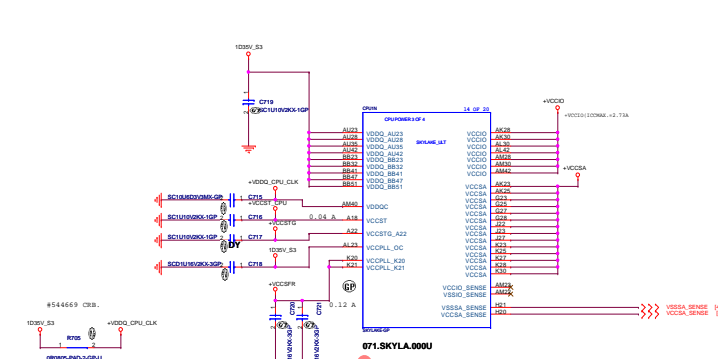
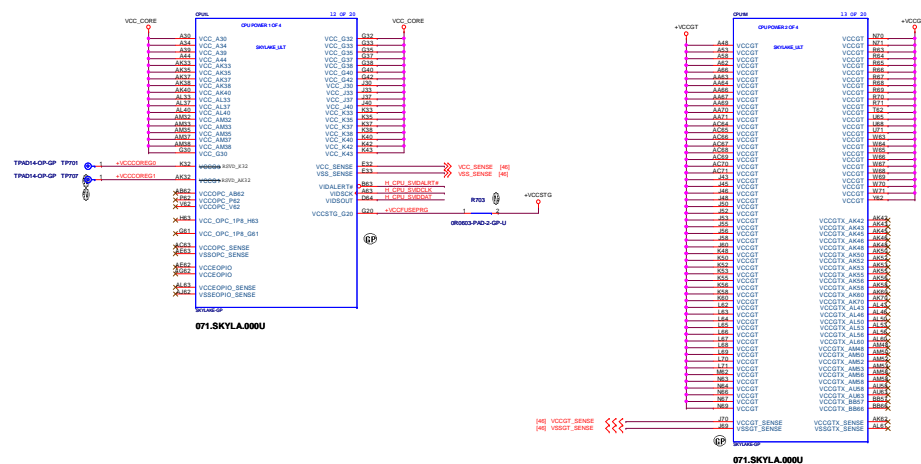
<Core Design>



Title	CPU_ (JTAG/CPU SIDE BAND)
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Size A3	Document Number Cottonwood SKL-U	Rev A00
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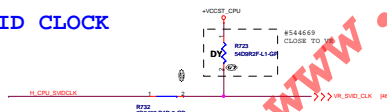


Layout Note:
1. Place close to CPU
2. VCC_SENSE / VSS_SENSE
Impedance=50 ohm
3. Length match=25m1

SVID DATA



SVID CLOCK



SVID_543016:

Figure 10-7. Routing Illustration for SVID Topology

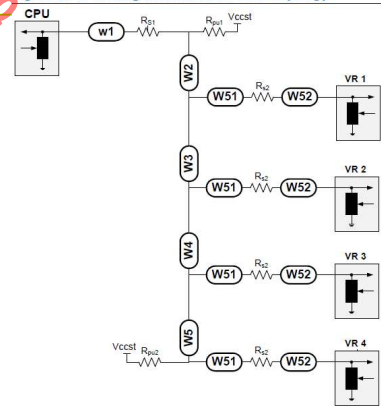
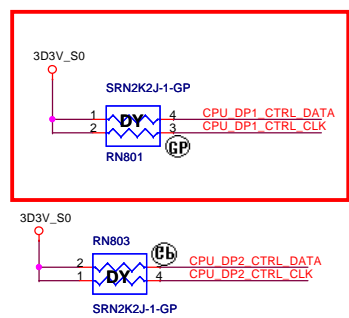


Table 10-10. SVID Bus Routing Guidelines

Signal	W1 [inches]	W2 [inches]	W3/4/5 [inches]	W2+W3+W4+W5 [inches]	W1 [inches]	W2 [inches]	R _{pull} [ohms]	R _{pull} [ohms]	R _{pull} [ohms]	R _{pull} [ohms]	V _{CC} [V]
VIDSOUT							100	100	0	10	
VIDSCK	0.5-3	1-15	0.5-4	3-17	<0.1	<0.1	Empty	45	0	50	1.0
VIDALERT							56	Empty	220	0	

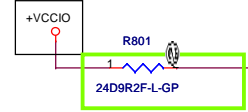
Dummy, Vendor suggest
20141117



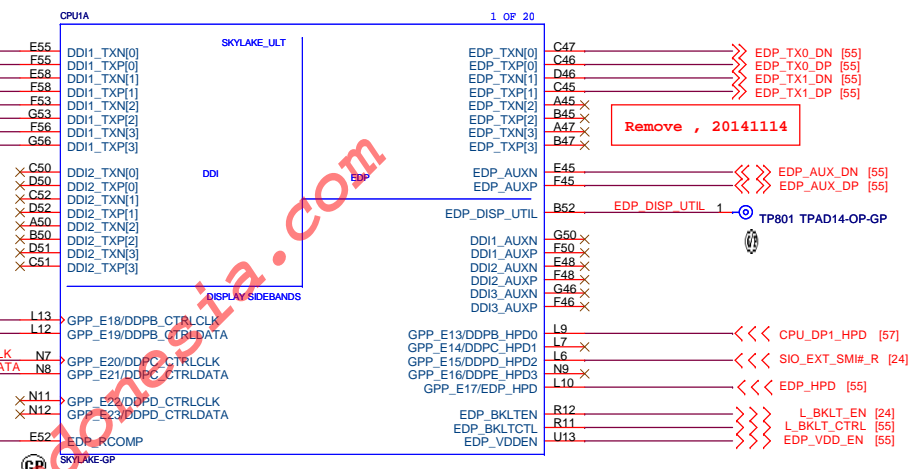
HDMI

HDMI

Check



[57] HDMI_DATA2#
[57] HDMI_DATA2
[57] HDMI_DATA1#
[57] HDMI_DATA1
[57] HDMI_DATA0#
[57] HDMI_DATA0
[57] HDMI_CLK#
[57] HDMI_CLK



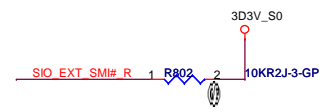
071.SKYLA.000U
(#543016) The Skylake U/Y processor supports only two DDI ports - Port 1 and Port 2.

(#543016) eDP_RCOMP Guideline

Signal	Trace Width	Isolation Spacing	Resistor Value	Length
eDP_RCOMP	20 mils	25 mils	24.9 Ω $\pm 1\%$	Max = 100 mils

(#543016) DDI Disabling and Termination Guidelines

Port	Strap	Enable Port	Disable Port
Port 1	DDPB_CTRLDATA	PU to 3.3 V with 2.2-k $\pm 5\%$ resistor	NC
Port 2	DDPC_CTRLDATA	PU to 3.3 V with 2.2-k $\pm 5\%$ resistor	NC



Design Guideline:
Skylake processor signal eDP_RCOMP should be connected to the VCCIO rail via a single 24.9 Ω $\pm 1\%$ resistor.

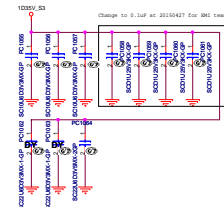
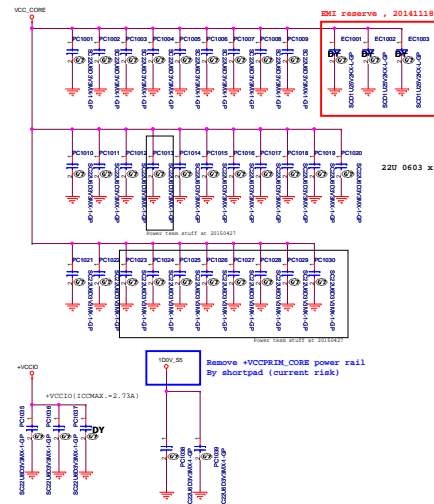
Main Func = CPU

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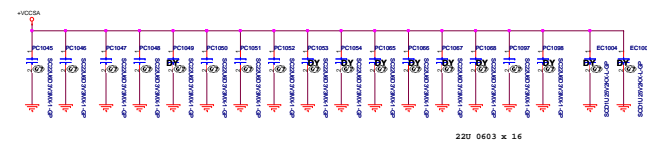
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CORE

U-line 23e 28W
IccMax current-10ms max = 34 A



VCCSA



SLICED GT

U-line 23e 28W
IccMax current-10ms max[A] = 67 A

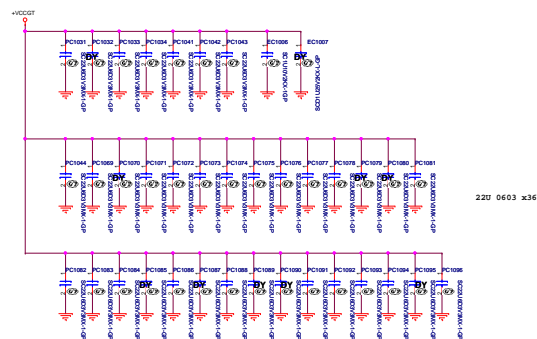


Table 53-3. SKL U Bulk Decoupling Requirements

Bulk Decoupling Locations		
Bulk Decoupling Locations	Requirements	Notes
VCC Power Plane at VR output	1x 220uF (±4.5mΩ ESR) 1x 100uF (±4.5mΩ ESR)	Placed at primary side near to VR output Placed at backside side near to VR output
VCGT Power Plane at VR output	1x 220uF (±4.5mΩ ESR)	Placed at primary side near to VR output Additional components needed when supporting 2.3e
VCGT ₂ Power Plane at VR output	1x 220uF (±4.5mΩ ESR)	Placed at primary side near to VR output Only needed when supporting 2.3e
VCCSO Power Plane at VR output	2x 47uF 0805	Placed at primary side near to VR output
VCCSO Power Plane at VR output	2x 47uF 0805	Placed at primary side near to VR output

Note: These requirements are based on 1MHz switching frequency VR with bandwidth of up to 250kHz.

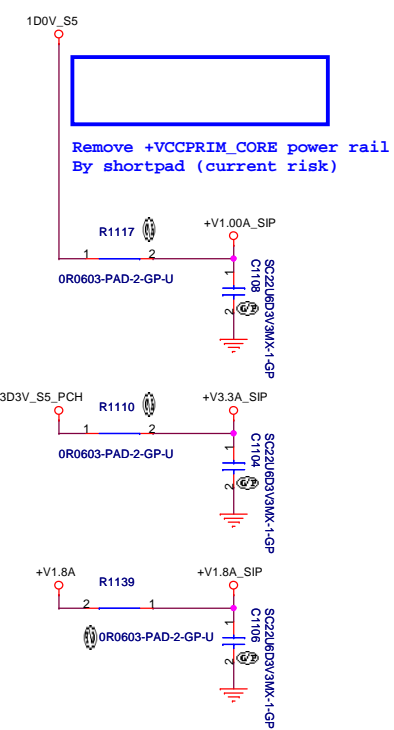
Table 53-4. Decoupling Requirements for SKL U Processor (Sheet 1 of 2)

Domain	Backside cap	Primary side cap	Placement guideline
VCC	9x 22uF 0603 7x 10uF 0402 15x 1uF 0201		Place on secondary side, underneath the package
		8x 41uF 0805 (6.3V)	Place as close to the package as possible
		8x 10uF 0402	
VGGT	10x 10uF 0402 12x 1uF 0201		Place on secondary side, underneath the package
		3x 47uF 0805 (6.3V)	Place as close to the package as possible
		7x 22uF 0603	
		3x 47uF 0805	Place as close to the package as possible
		5x 22uF 0603	Additional components needed when supporting 23e
VGGTX	8x 10uF 0402		Place on secondary side, underneath the package Only needed when supporting 23e
		8x 22uF 0603	Only needed when supporting 23e
VCGSA	7x 10uF 0402 7x 1uF 0201		Place on secondary side, underneath the package
		6x 10uF 0402	Place as close to the package as possible
VCCIO	2x 10uF 0402 4x 1uF 0201		Place on secondary side, underneath the package
		4x 1uF 0402	Place as close to the package as possible
VDDQ	2x 10uF 0402 4x 1uF 0201		Place on secondary side, underneath the package
		4x 10uF 0402	Place as close to the package as possible
VDDQC	1x 1uF 0201		Place on secondary side, underneath the package
VCCPLL	1x 10uF 0402		Place as close to the package as possible
VCCST	1x 1uF 0402		Place as close to the package as possible

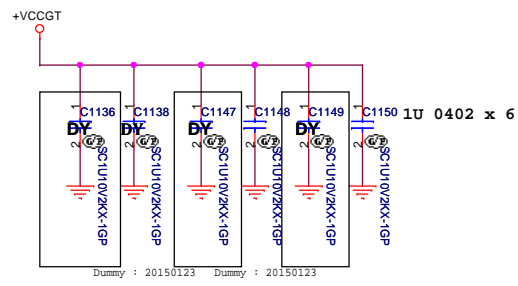
Table 53-4. Decoupling Requirements for SKL U Processor (Sheet 2 of 2)

Domain	Backside cap	Primary side cap	Placement guideline
VCCSTG	1x 1uF 0402		Place on secondary side, underneath the package Placeholder only
VCCCEPIO	2x 10uF 0402		Place on secondary side, underneath the package
VCCOPC	1x 10uF 0402		Place on secondary side, underneath the package
	6x 1uF 0501		

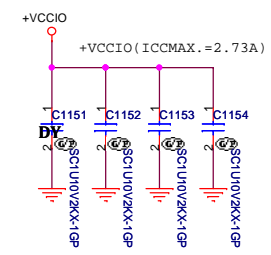
PCH DERIVED RAILS



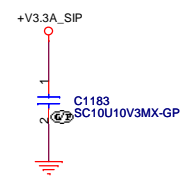
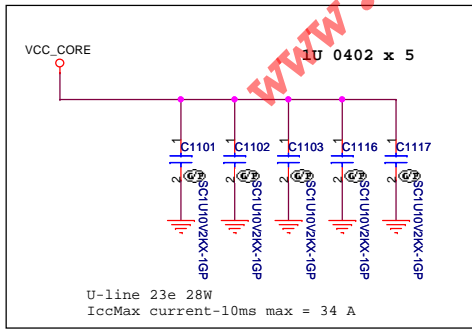
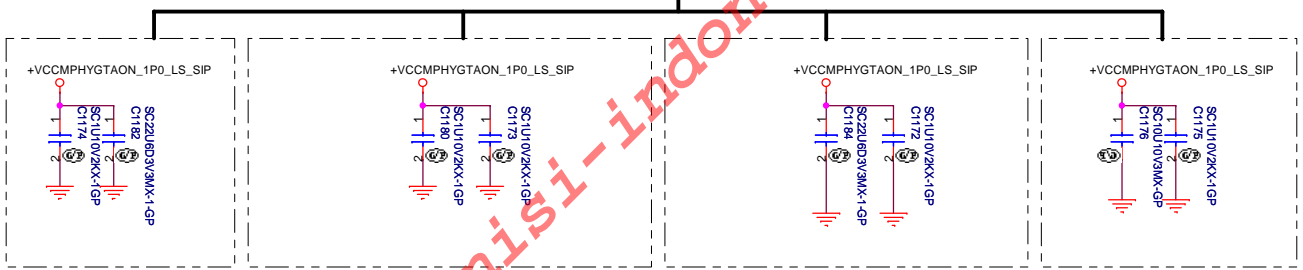
UNSLICED GT

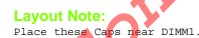
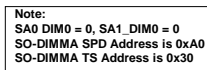
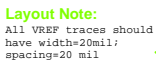


VCCIO



+VCCMPHYGTAON_1P0 (ICCMAX.=2.12A)






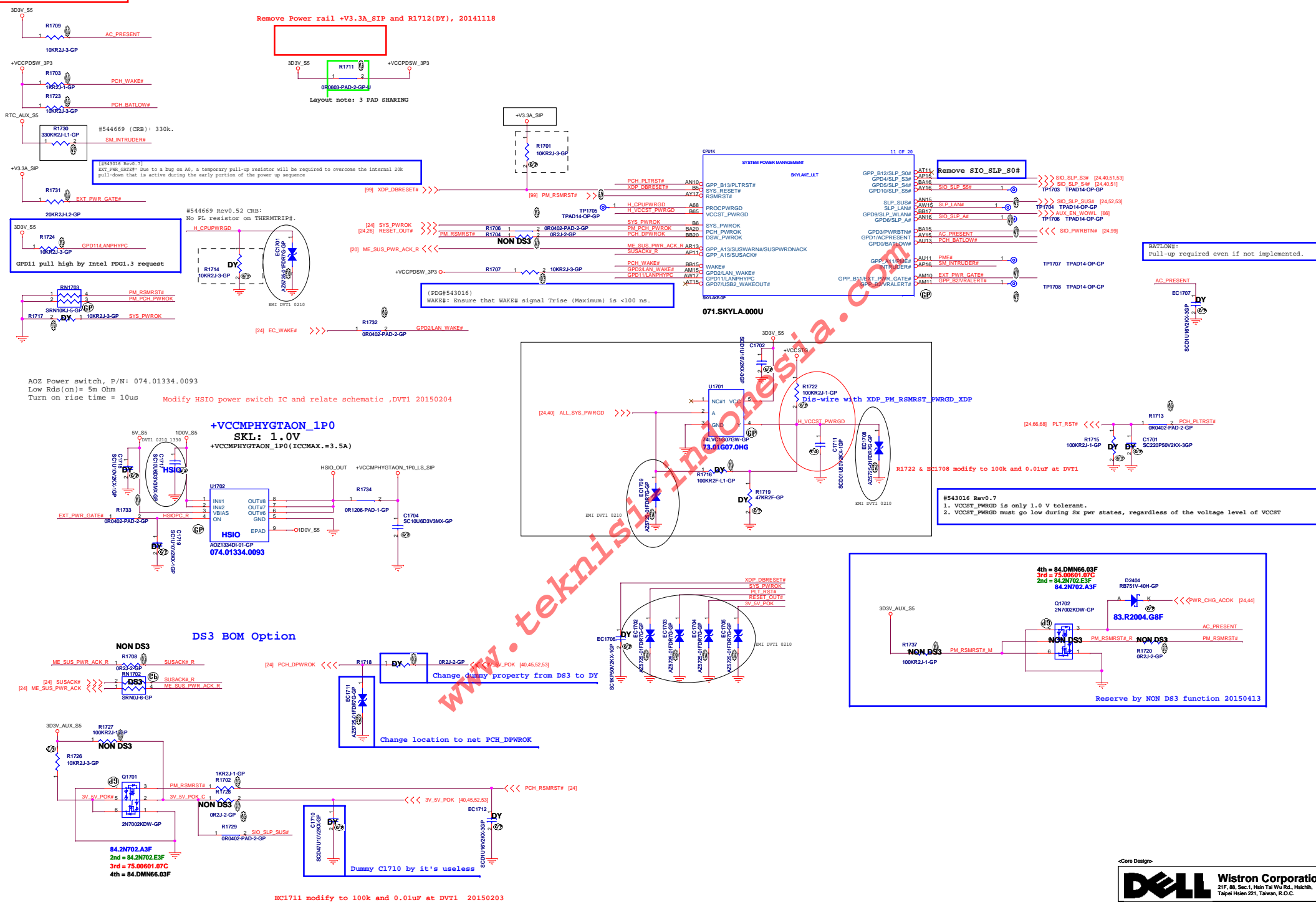
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5
Main Func = PCH



Main Func = PCH

Strap pin:

Port B / Port C Detected	Sampled at rising edge of PCH_PWROK
DDPB_CTRLDATA	0 = Port B is not detected. ★ 1 = Port B is detected.
DDPC_CTRLDATA	0 = Port C is not detected. ★ 1 = Port C is detected.

These two signals have weak internal pull-down.

PCH strap pin:

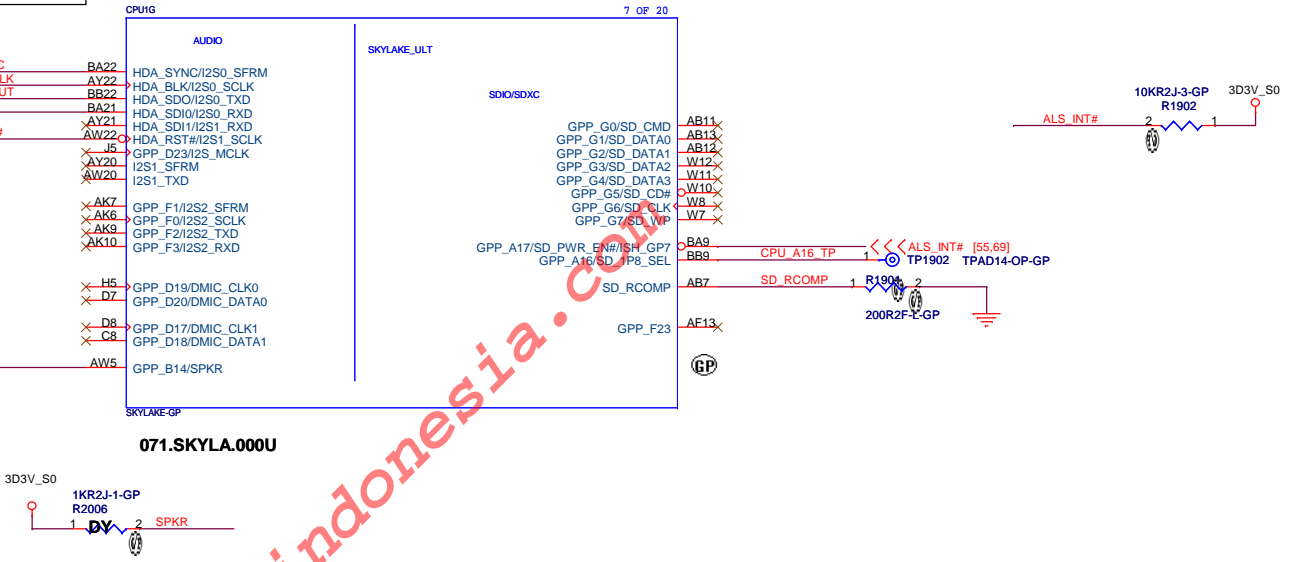
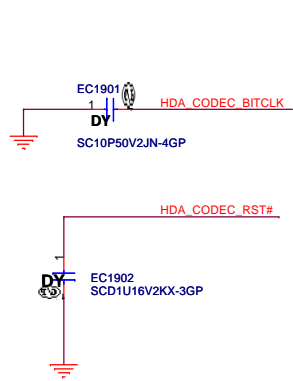
Flash Descriptor Security Override/ Intel ME Debug Mode	
HDA_SDOUT	Low = Default ★ High = Enable

The internal pull-down is disabled after PLTRST# deasserts

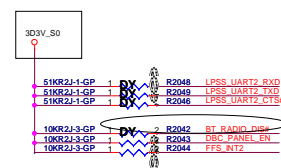
PCH strap pin:

NO REBOOT	
HDA_SPKR	★ Low = Enable (Default) High = Disable

The internal pull-down is disabled after PLTRST# deasserts



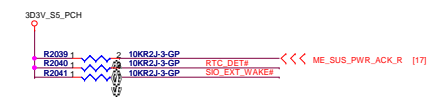
Main Func = PCH

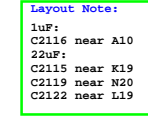
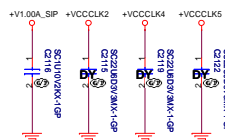
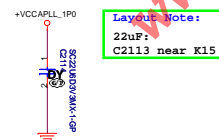
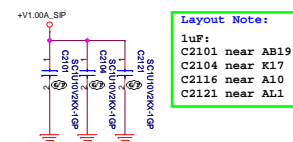
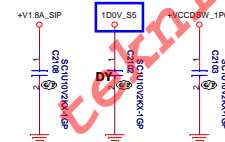
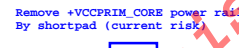
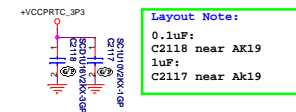


PCH strap pin:

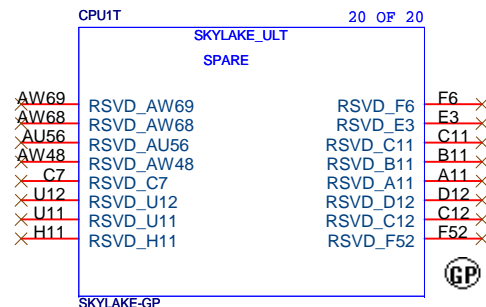
No Reboot	Sampled at rising edge of PCH_PWROK
GSP10_MOSI / GPP_B18	0 = Disable "No Reboot" mode. 1 = Enable "No Reboot" mode (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

The signal has a weak internal pull-down.





Main Func = PCH



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Title

CPU (RSVD)

Size
A4

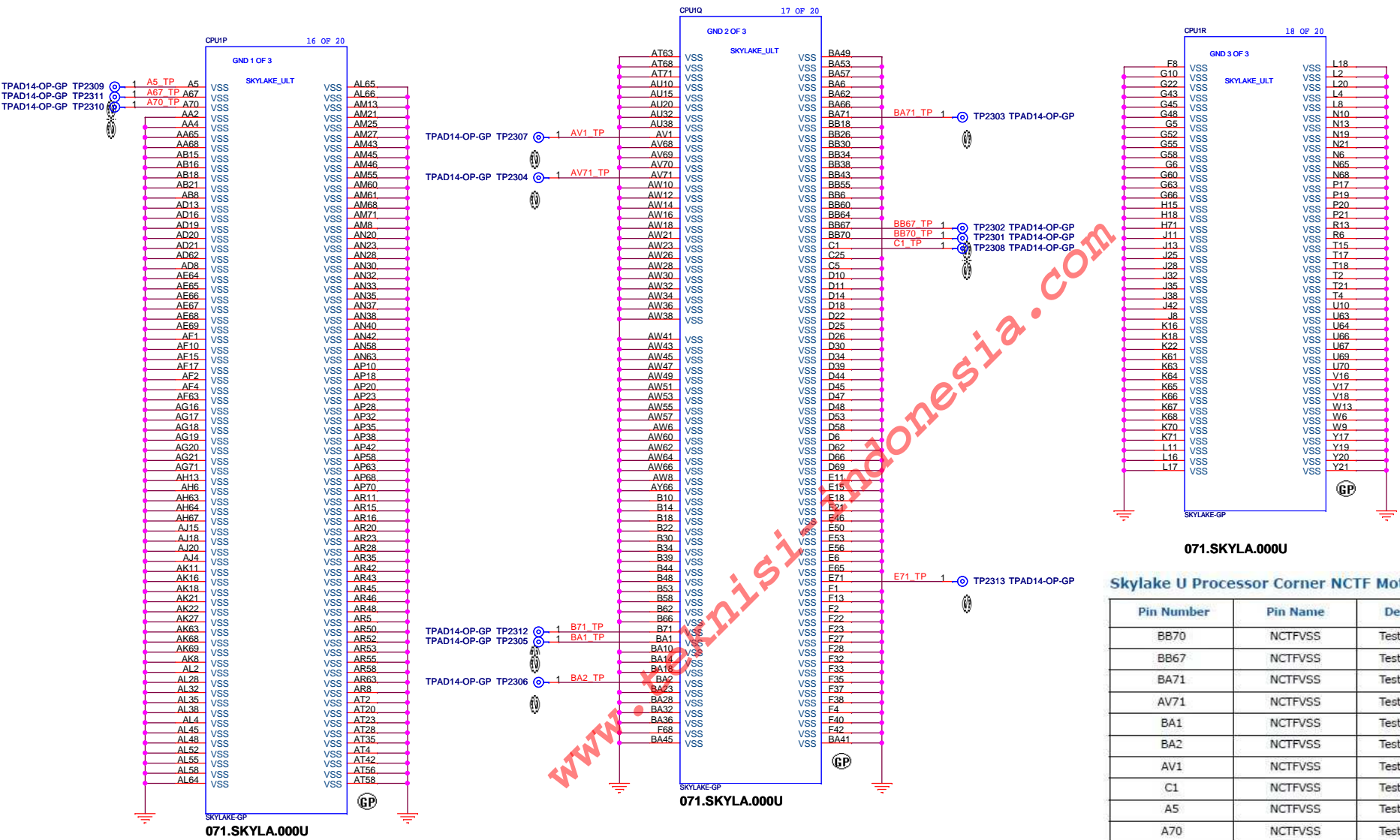
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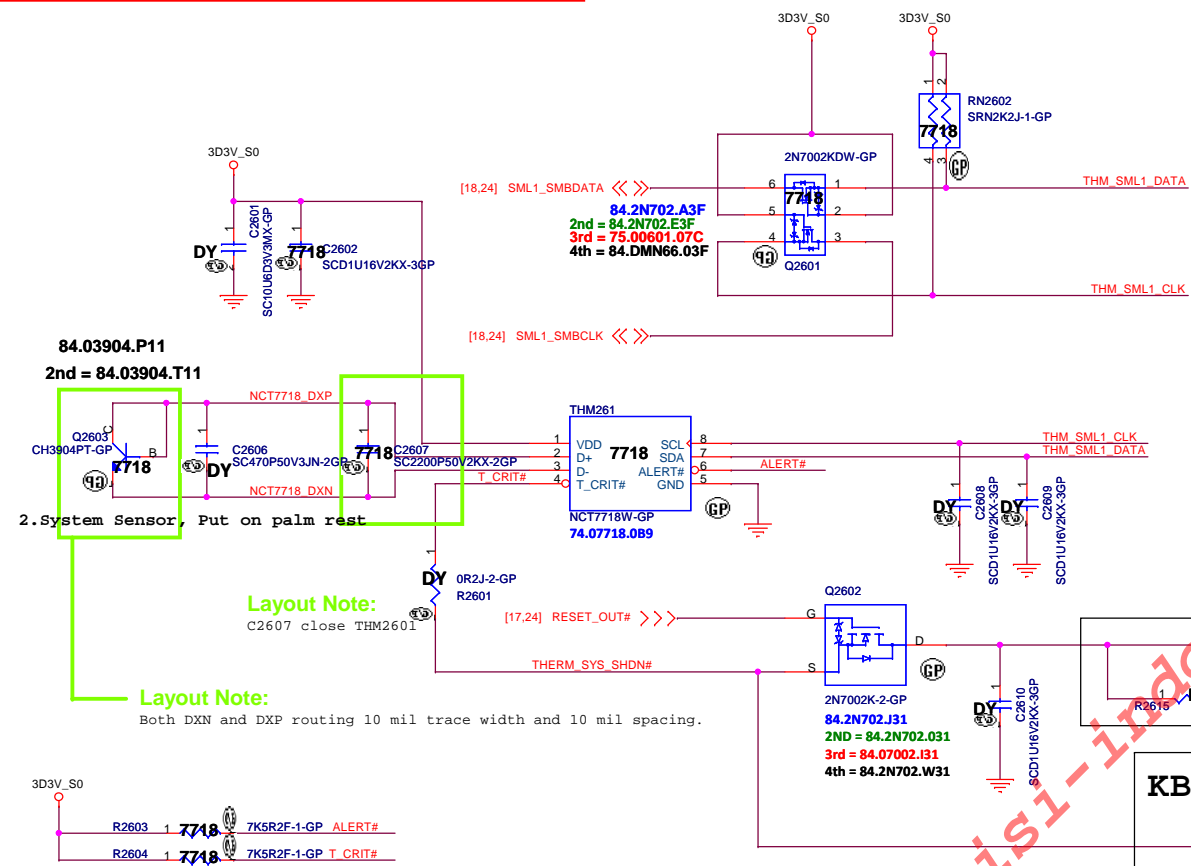
Skylake U Processor Corner NCTF Motherboard Test Point Example

Pin Number	Pin Name	Description	Corner
BB70	NCTFVSS	Test Point (TP)	Corner BB71
BB67	NCTFVSS	Test Point (TP)	
BA71	NCTFVSS	Test Point (TP)	
AV71	NCTFVSS	Test Point (TP)	Corner BB1
BA1	NCTFVSS	Test Point (TP)	
BA2	NCTFVSS	Test Point (TP)	
AV1	NCTFVSS	Test Point (TP)	Corner A1
C1	NCTFVSS	Test Point (TP)	
A5	NCTFVSS	Test Point (TP)	
A70	NCTFVSS	Test Point (TP)	Corner A71
A67	NCTFVSS	Test Point (TP)	
B71	NCTFVSS	Test Point (TP)	
E71	NCTFVSS	Test Point (TP)	

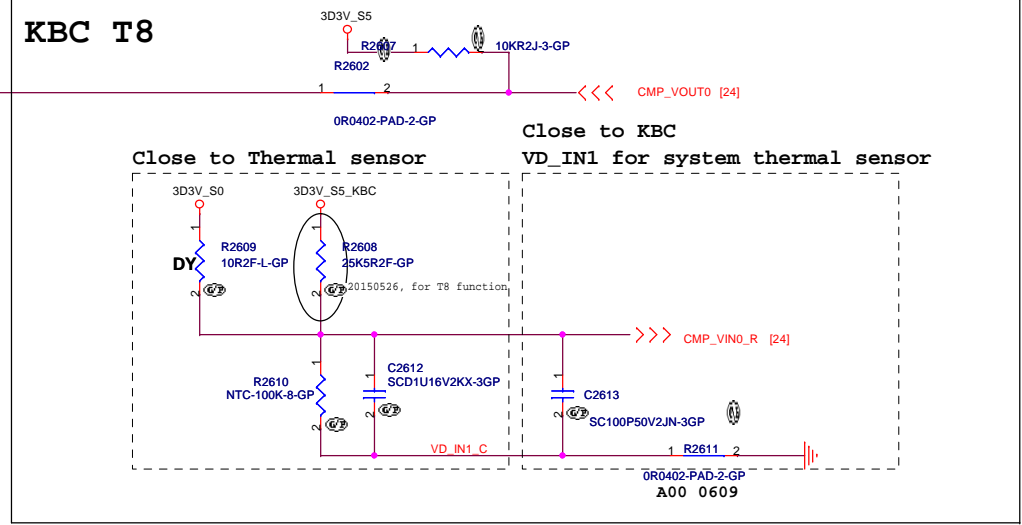
20140814 DAVID



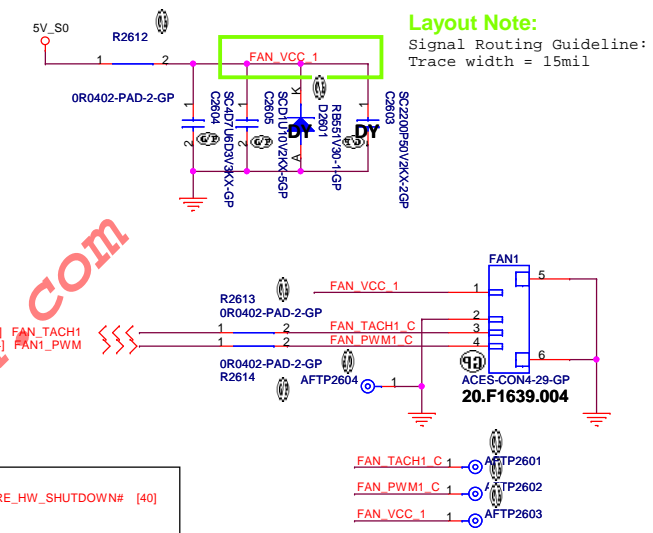
Main Func = Thermal Sensor



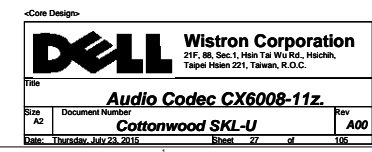
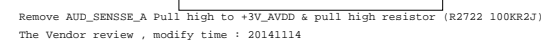
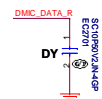
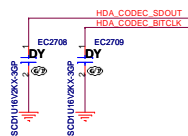
TEMPERATURE (°C)		T_CRIT#				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125



PWM FAN1



Layout Note:
Signal Routing Guideline:
Trace width = 15mil



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Main Func = Audio

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Main Func = LAN

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A2

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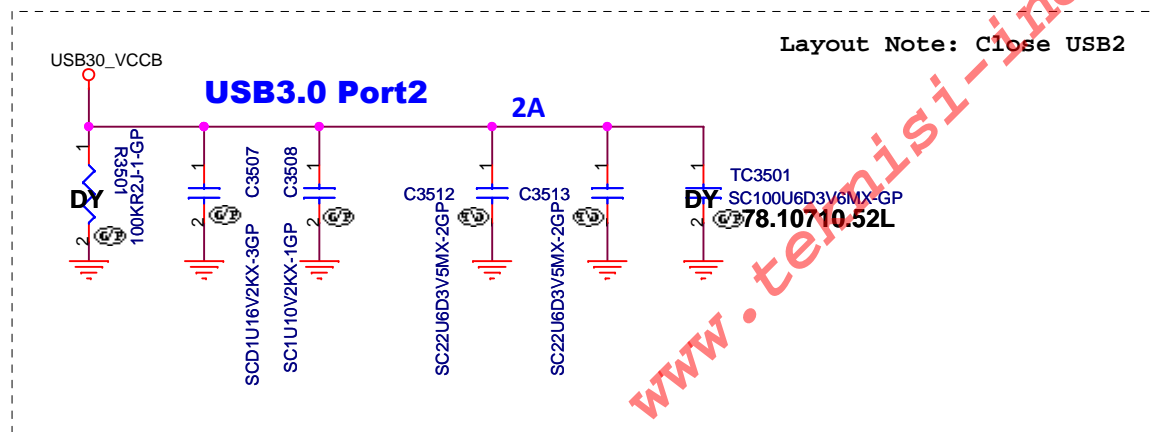
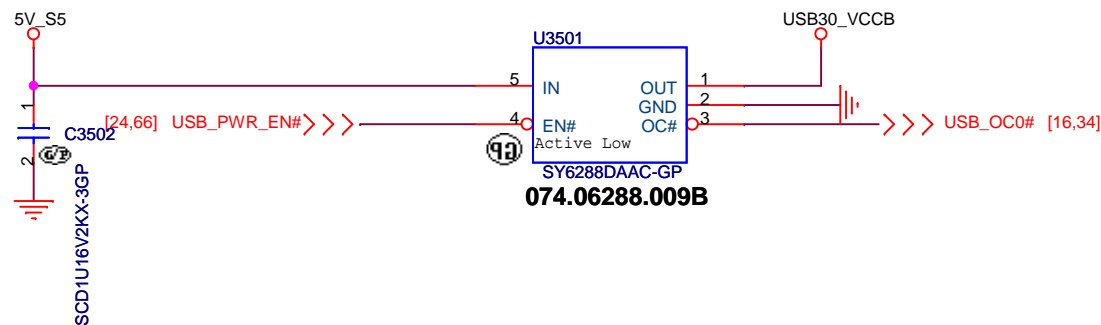
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Main Func = Card Reader

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Main Func = USB3.0 Port1



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Title

USB switch

Size	Document Number
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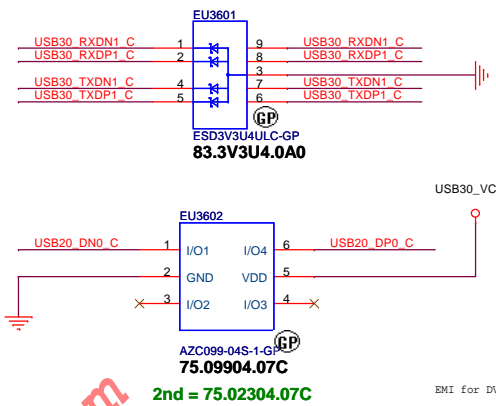
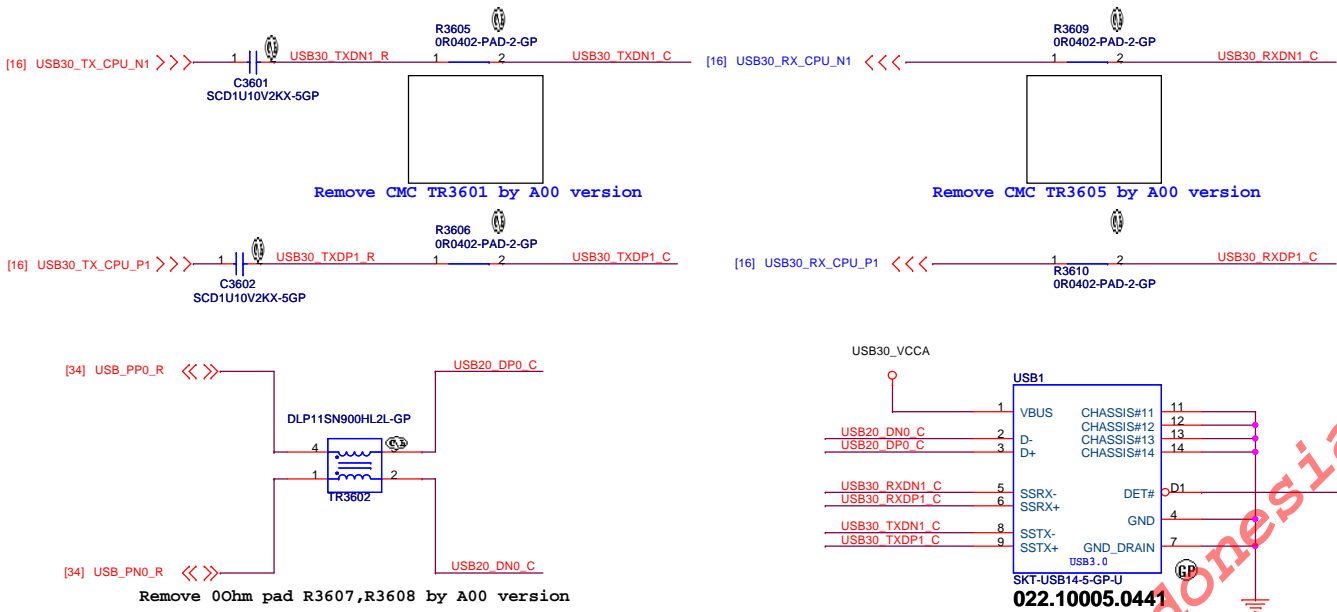
Date: Wednesday, July 08, 2015

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Main Func = USB3.0 Port1

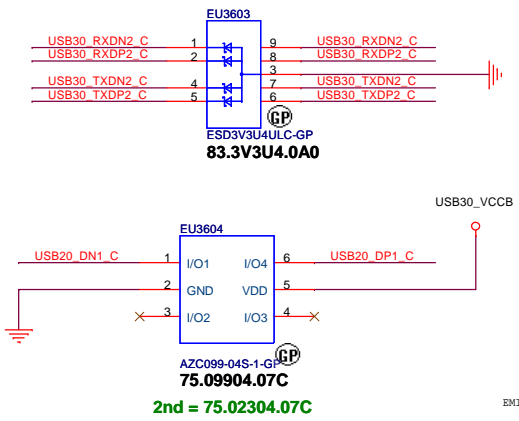
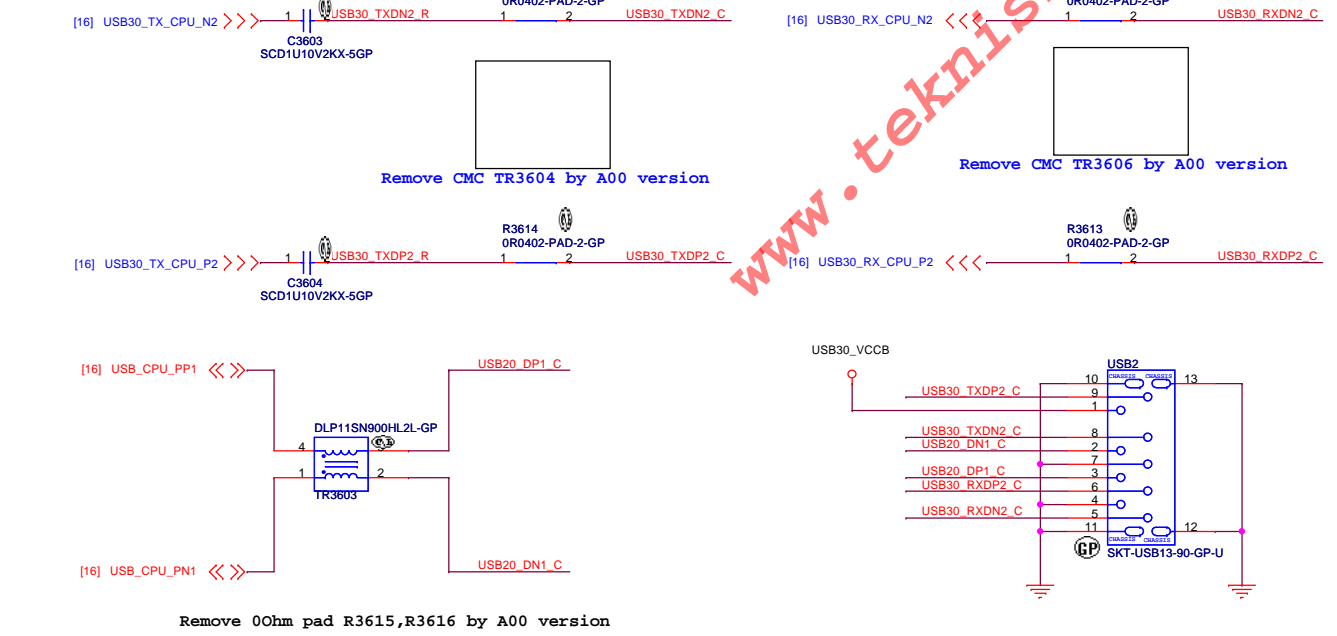
USB2.0 Port2 and USB2.0 Port3 are on IOBD

USB3.0 Port1



USB 3.0 Connector Pin definition	
1	POWER
2	USB 2.0 D-
3	USB 2.0 D+
4	GND
5	StdA_SSRX- SuperSpeed RX
6	StdA_SSRX+
7	GND
8	StdA_SSTX- SuperSpeed TX
9	StdA_SSTX+

USB3.0 Port2



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Title: **USB30**

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Main Func = USB2.0

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Main Func = USB3.0 Port1

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(Reserved)

Size
A4

Document Number
Cottonwood SKL-U

Rev
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Main Func = USB3.0 Port1

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Title

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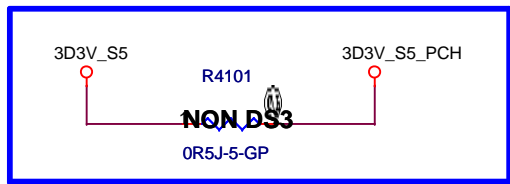
Size
A4

Document Number
Cottonwood SKL-U

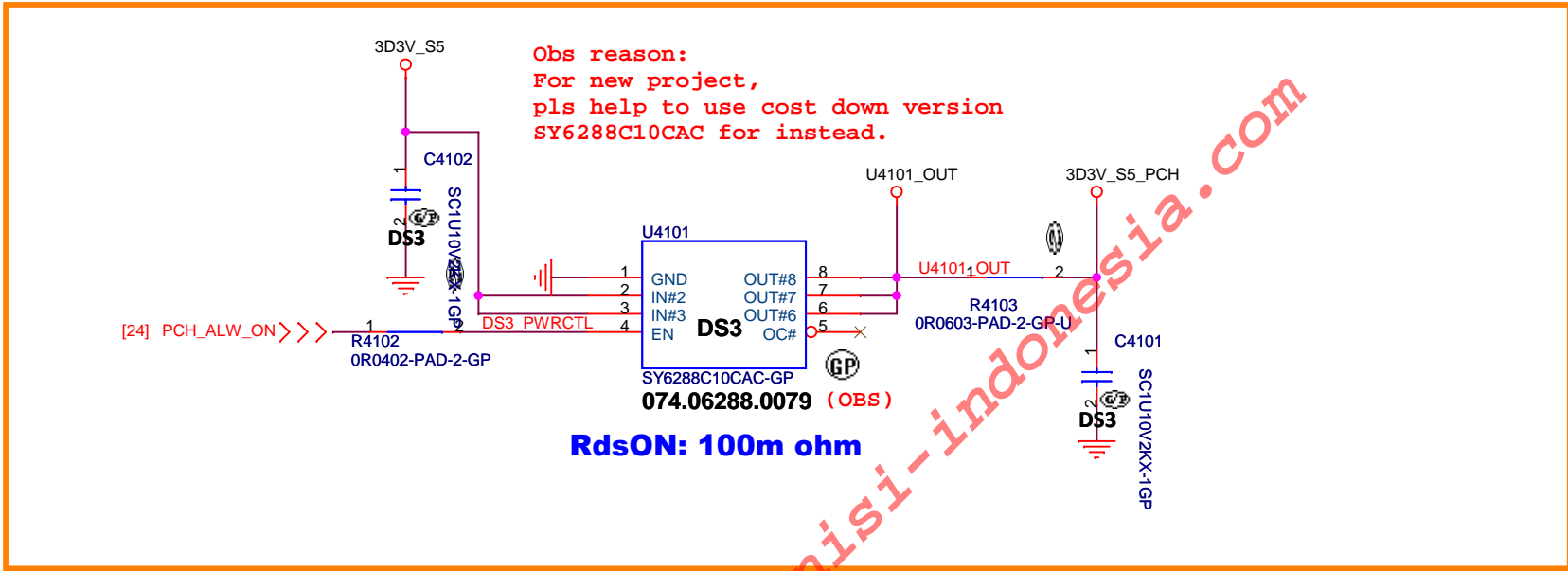
Rev
A00

Date: Wednesday, July 08, 2015Sheet 39 of 105

Main Func = Power Plane & Sequence



Reserve by NON DS3 function 20150413




Obs reason:
For new project,
pls help to use cost down version
SY6288C10CAC for instead.

RdsON: 100m ohm

DS3

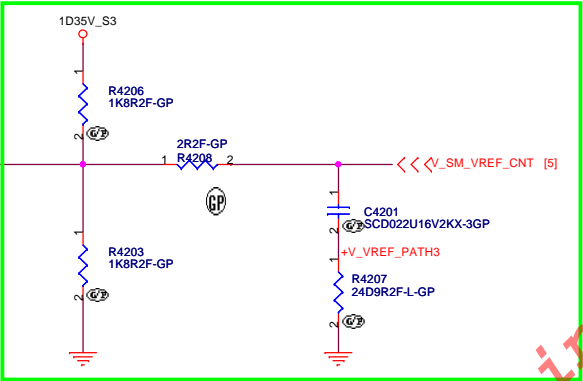
<Core Design>

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Title Connected_Standby(1/2)+DS3			
Size A4	Document Number Cottonwood SKL-U		Rev A00
Date: Thursday, July 09, 2015		Sheet 41 of	105

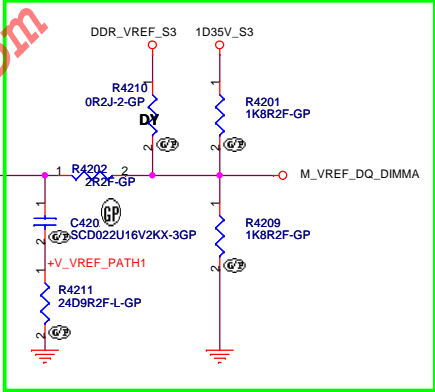
Main Func = DIMM1
Main Func = DIMM2

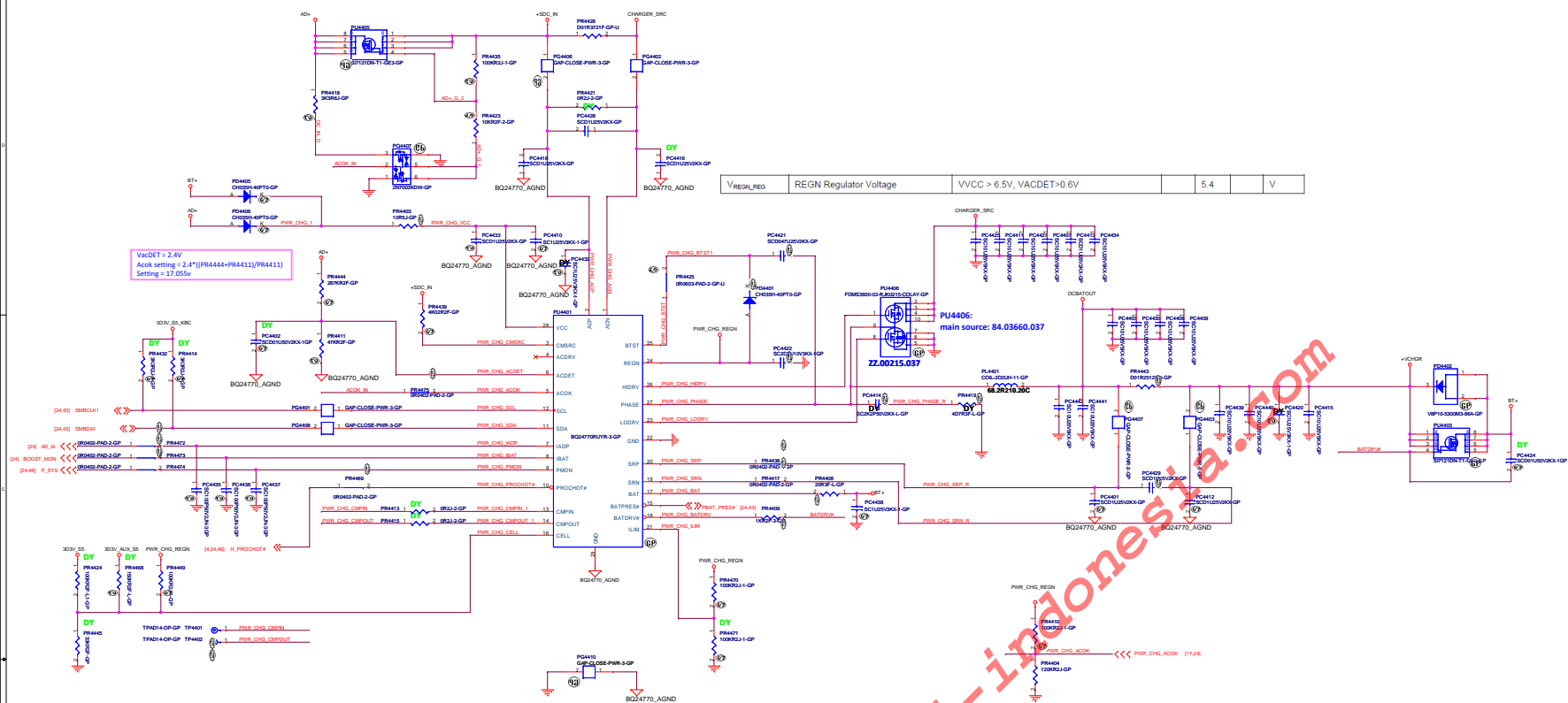
VREF CIRCUITRY

Layout Note:
Place Close DIMMs



Layout Note:
Place Close DIMM1



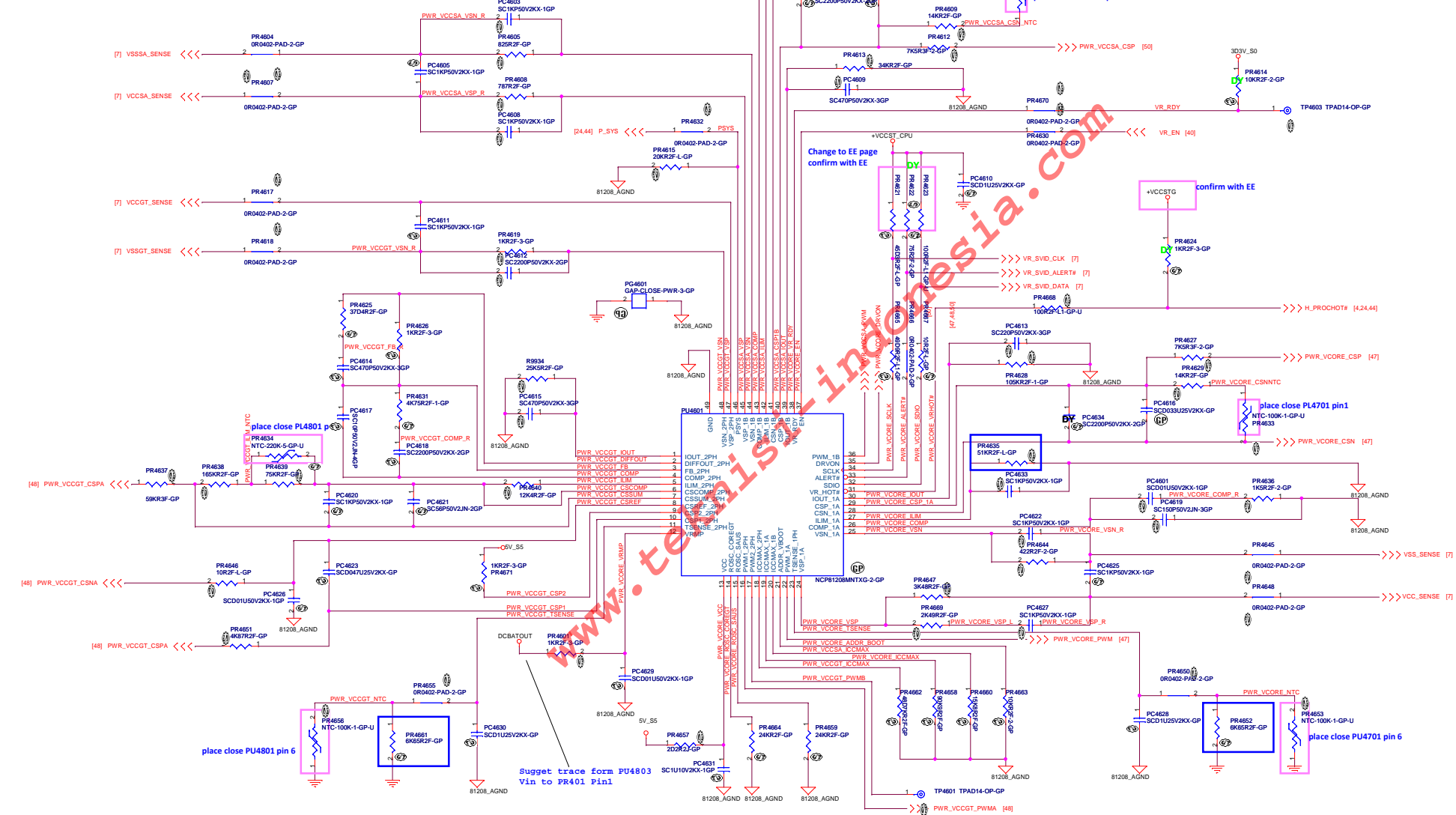


Remove PQ4405 relate schematic , 20141118

Main Func = CPU_CORE

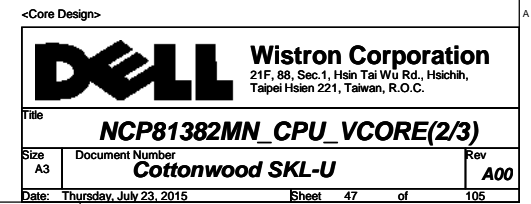
SKU	TDP[W]	Core+Ring+LLC	GT	GTx	SA	VCCI	VCCST	VCCDDQ	VCCOPC	VCCE0P10
SKL-Y(2+2)	4	16	20	N/A	4.1	3	0.1	2	N/A	N/A
SKL-U (2+2)	15	28	31	N/A	4.5	3	0.075	2	NA	N/A
SKL-U (2+3e, 64MB)	15	29	57	7	5.1	3.1	0.12	2	3	3
	28	29	57	7	5.1	3.1	0.12	2	3	3

SKU	TDP [W]	Turbo Power [W]	TDC Core+Ring+LLC [A]	TDC GT [A]	TDC GTx [A]	TDC SA [A]
SKL-Y	4	14	12	11	N/A	3.7
SKL-U (2+2)	15	29	21	10	N/A	3.7
	15	48	21	32	4	4.5
SKL-U (2+3e, 64 MB)	28	51	23	35	5	4.5



SKU	TDP[W]	Core+Ring+LLC	GT	GTx	SA	VCCI O	VCCST	VCCDDQ	VCCOPC	VCCEPIO
SKL-Y(2+2)	4	16	20	N/A	4.1	3	0.1	2	N/A	N/A
SKL-U (2+2)	15	28	31	N/A	4.5	3	0.075	2	NA	N/A
SKL-U (2+3e, 64MB)	15	29	57	7	5.1	3.1	0.12	2	3	3
	28	29	57	7	5.1	3.1	0.12	2	3	3

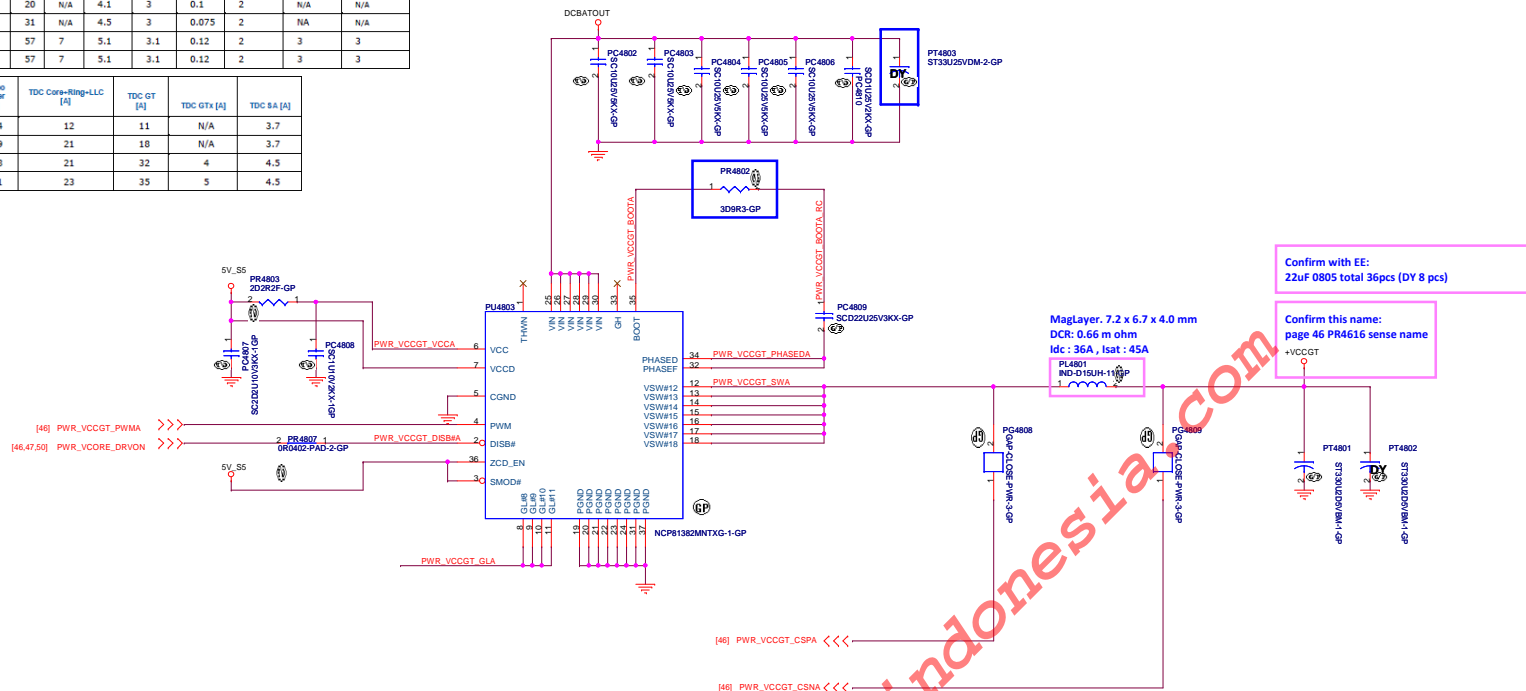
SKU	TDP [W]	Turbo Power [W]	TDC Core-Ring+LLC [A]	TDC GT [A]	TDC GTx [A]	TDC SA [A]
SKL-Y	4	14	12	11	N/A	3.7
SKL-U (2+2)	15	29	21	18	N/A	3.7
SKL-U (2+3e, 64 MB)	15	48	21	32	4	4.5
	28	51	23	35	5	4.5



```
Main Func = CPU_CORE
```

SKU	TDP[W]	Core+Ring+LLC	GT	GTx	SA	VCCl_O	VCCST	VCCDDQ	VCCOPC	VCCOEPIO
SKL-Y(2+2)	4	16	20	N/A	4.1	3	0.1	2	N/A	N/A
SKL-U (2+2)	15	28	31	N/A	4.5	3	0.075	2	N/A	N/A
SKL-U (2+3e, 64MB)	15	29	57	7	5.1	3.1	0.12	2	3	3
	28	29	57	7	5.1	3.1	0.12	2	3	3

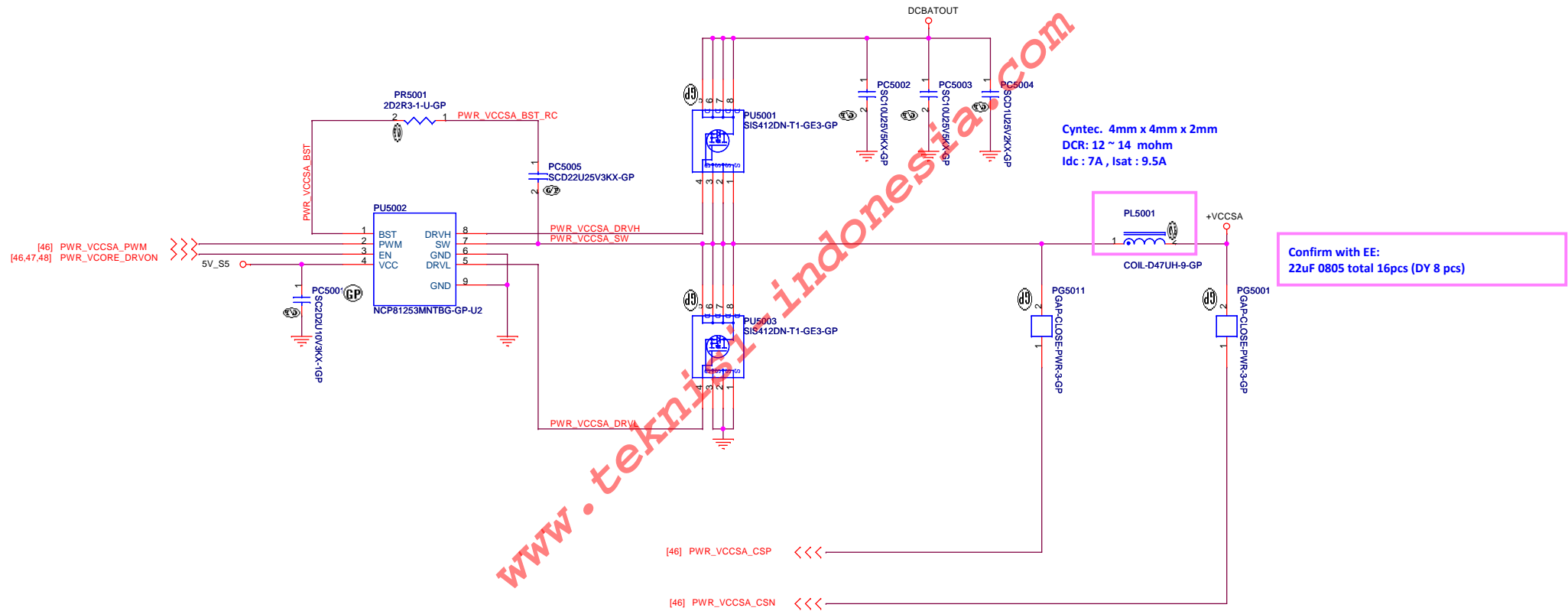
SKU	TDP [W]	Turbo Power [W]	TDC Core+Ring-L3C [A]	TDC GT [A]	TDC GTx [A]	TDC SA [A]
SKL-Y	4	14	12	11	N/A	3.7
SKL-U (2+2)	15	29	21	18	N/A	3.7
SKL-U (2+3e, 64 MB)	15	40	21	32	4	4.5
	28	51	23	35	5	4.5



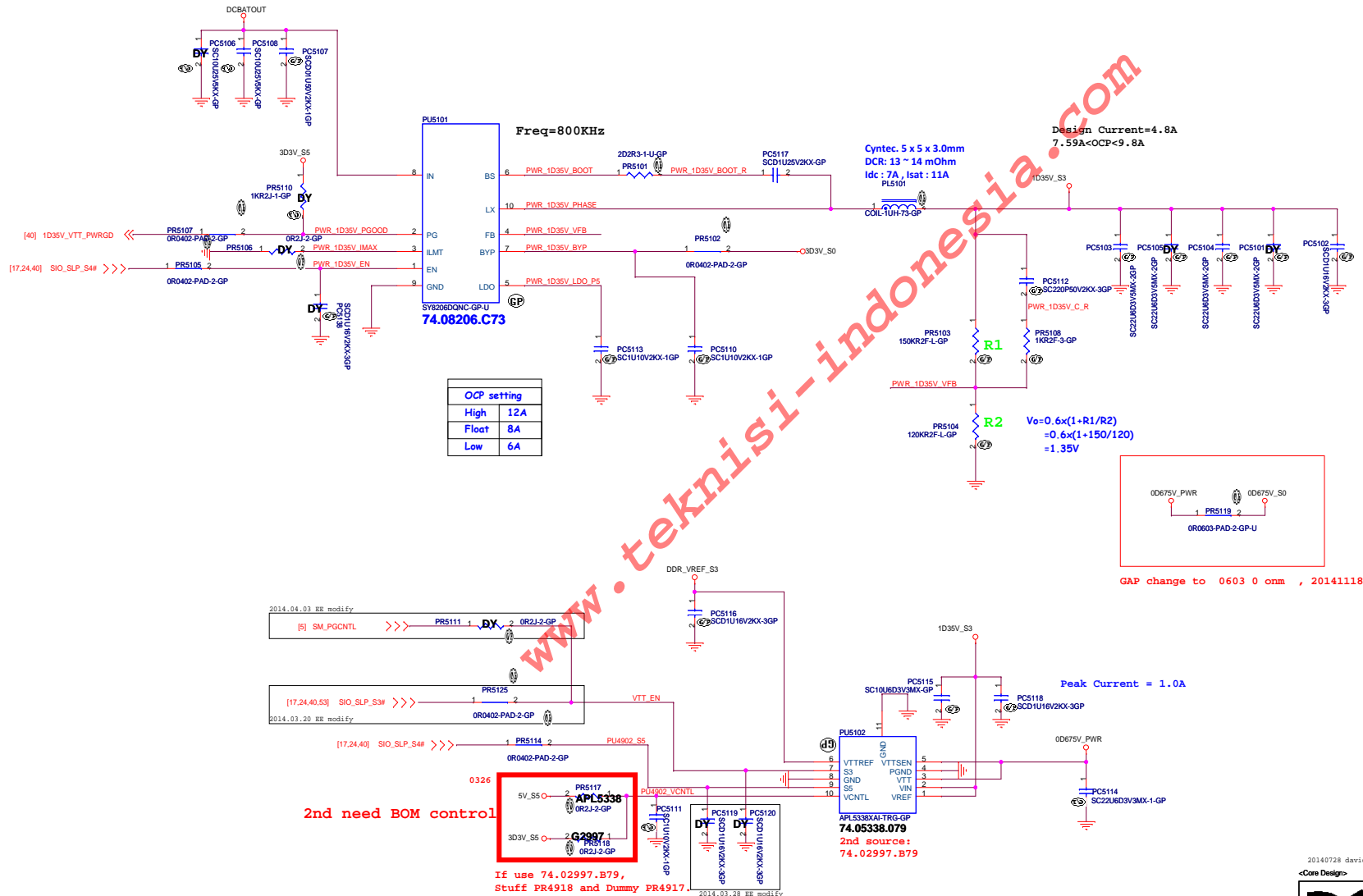
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SKU	TDP[W]	Core+Ring+LLC	GT	GTx	SA	VCCI O	VCCST	VCCDDQ	VCCOPC	VCCEOPIO
SKL-Y(2+2)	4	16	20	N/A	4.1	3	0.1	2	N/A	N/A
SKL-U (2+2)	15	28	31	N/A	4.5	3	0.075	2	NA	N/A
SKL-U (2+3e, 64MB)	15	29	57	7	5.1	3.1	0.12	2	3	3
	28	29	57	7	5.1	3.1	0.12	2	3	3

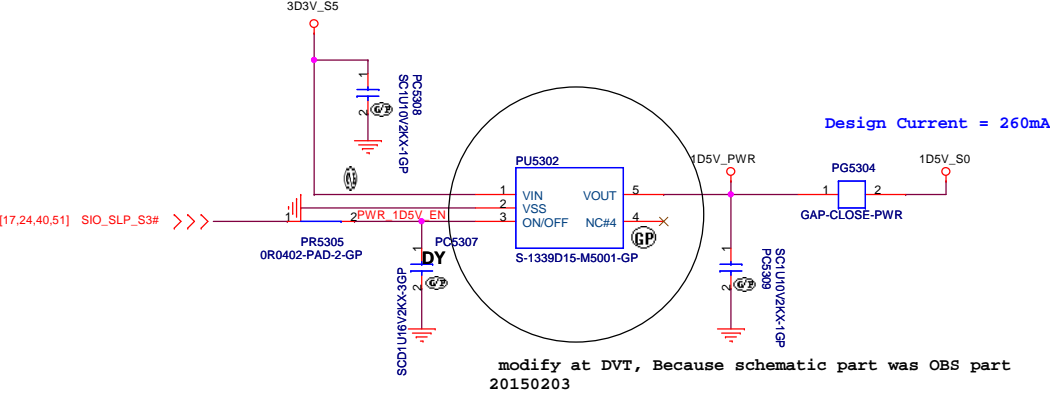
SKU	TDP [W]	Turbo Power [W]	TDC Core-Ring+LLC [A]	TDC GT [A]	TDC GTx [A]	TDC SA [A]
SKL-Y	4	14	12	11	N/A	3.7
SKL-U (2+2)	15	29	21	18	N/A	3.7
SKL-U (2+3e, 64 MB)	15	48	21	32	4	4.5
	28	51	23	35	5	4.5



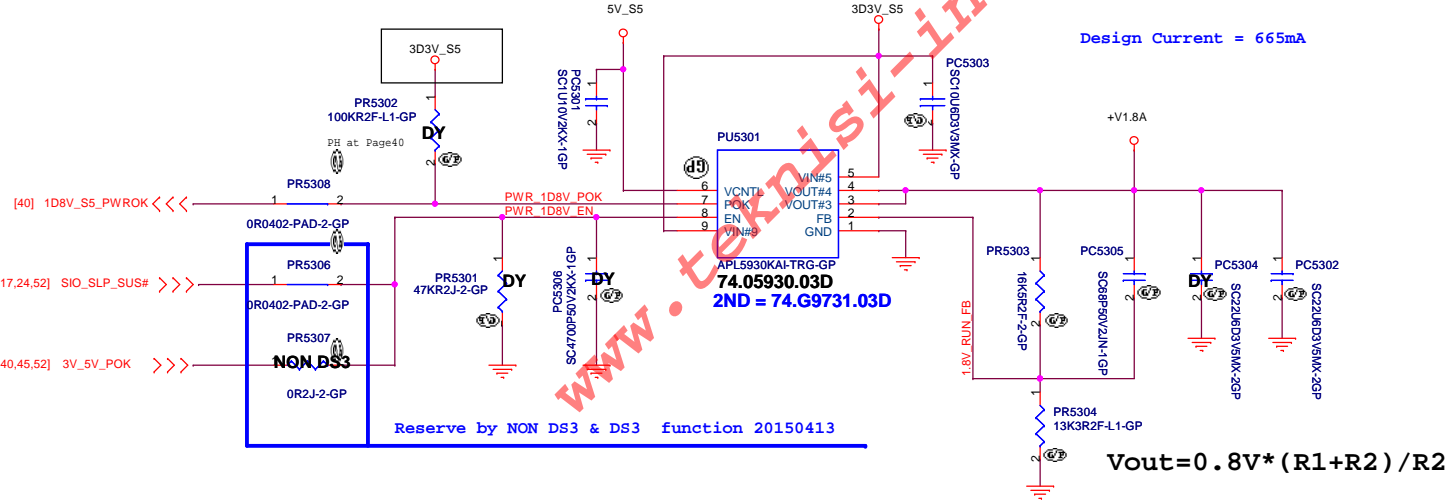
SY8206D for 1D35V



TLV70215 for 1D5V_S0



APL5930 for 1D8V_S5

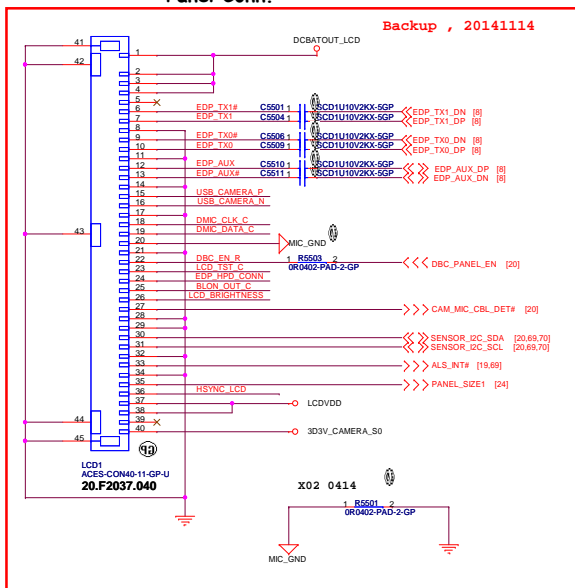


5	4	3	2	1
D				D
C				C
B				B
A				A

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<Variant Name>			
Title <Title>			
Size A	Document Number <Doc>		Rev A00
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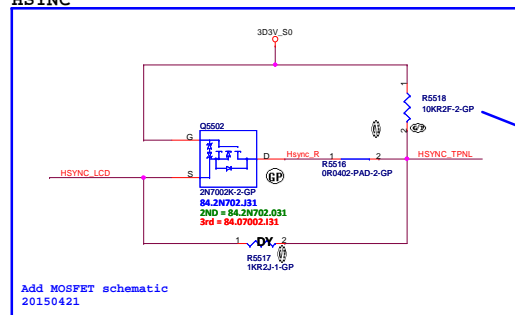
Panel Conn.



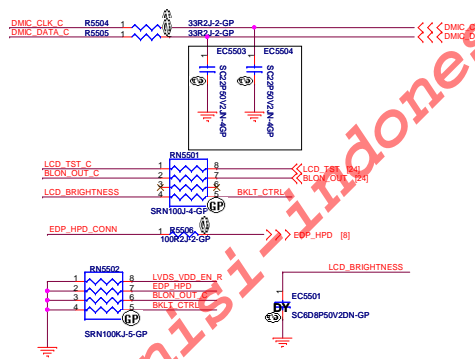
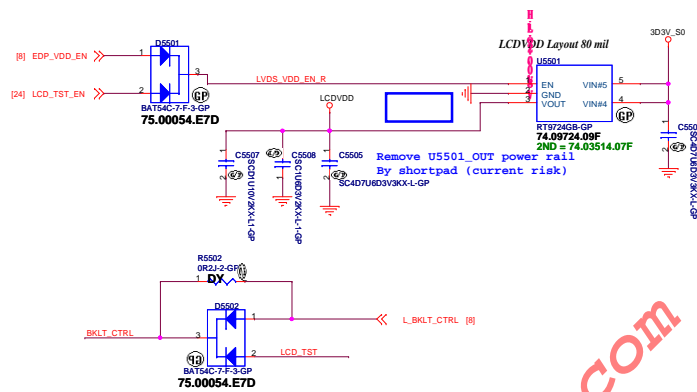
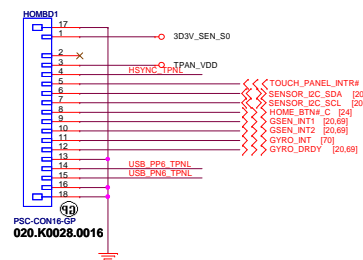
Power Pin Count : 7

GND Pin Count : 9

HSYNC



Change from 10k ohm (J) to 10k ohm (F)
20150423

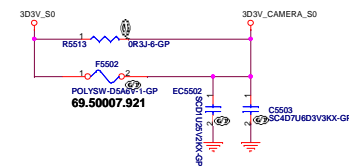


Remove 00hm pad R5508,R5509 by A00 version

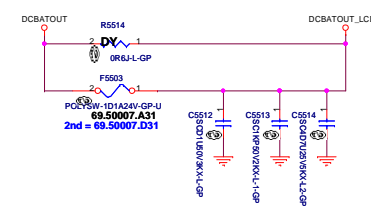
Remove CMC TR5502 by A00 version.

1 2 << >> USB_CPU_PP6 [16]

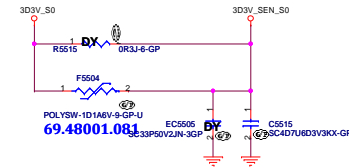
CAMERA POWER



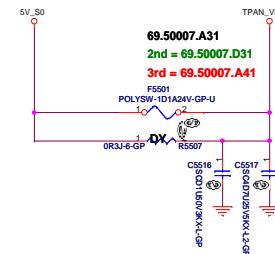
INVERTER POWER



SENSOR POWER

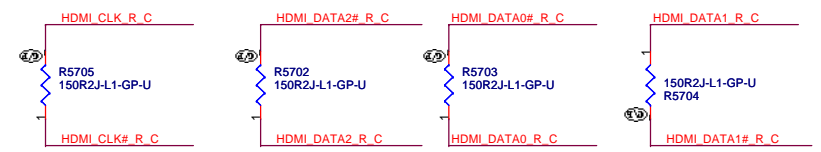
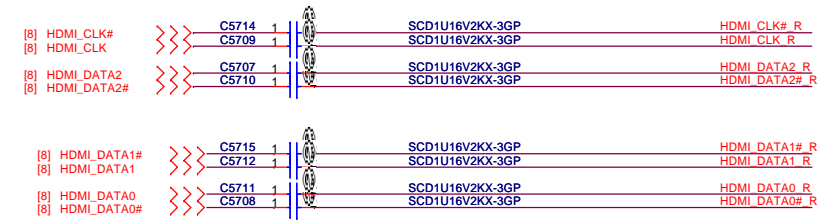


TOUCH PANEL POWER

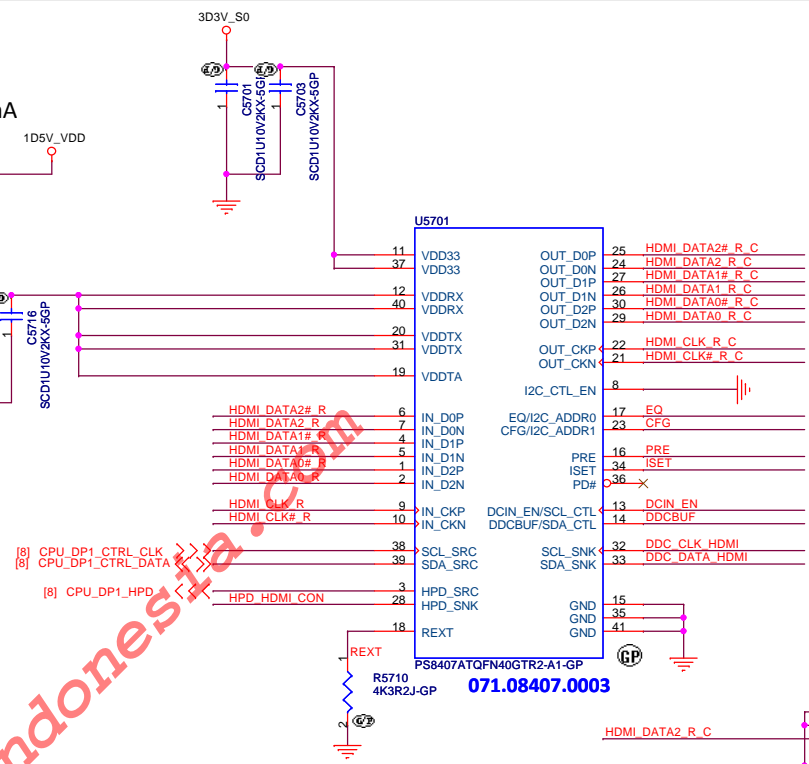
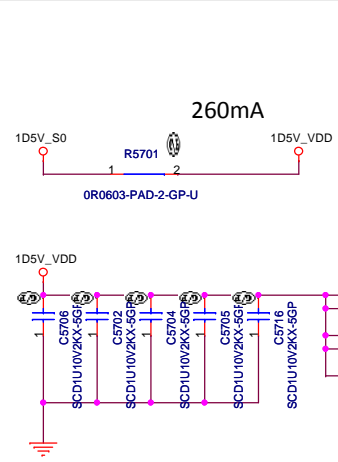
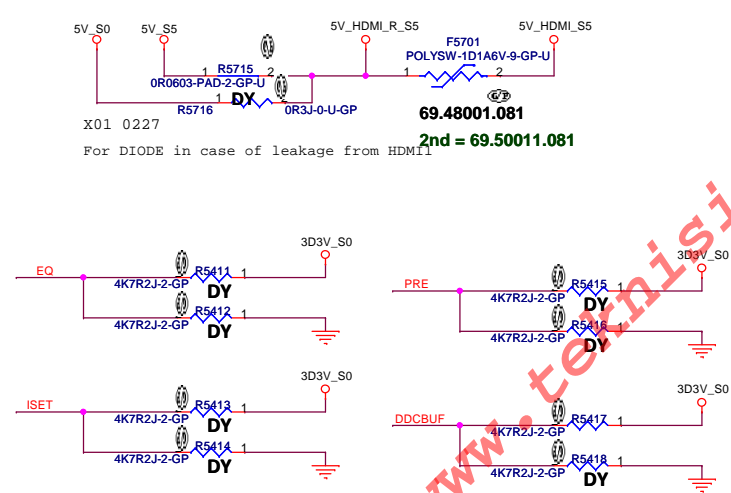
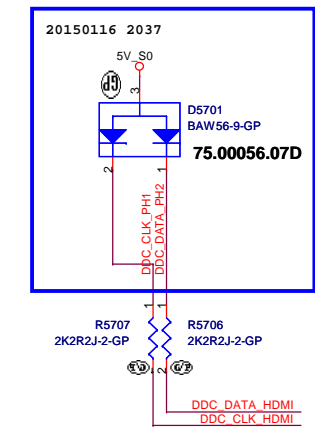


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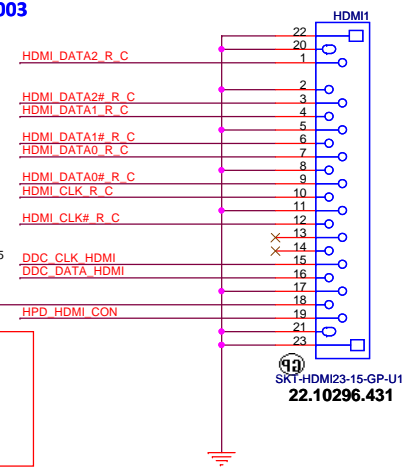
Main Func = HDMI



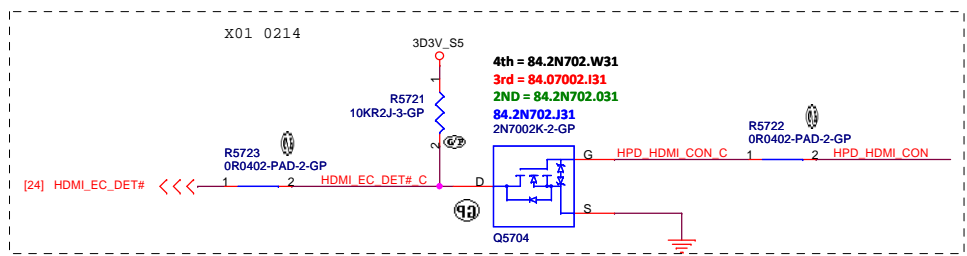
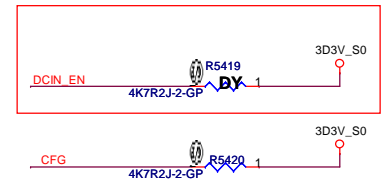
Change symbol part number, because origin symbol is DELL OBS part



HDMI CONN



Vendor suggest, Dummy for floating
20141117



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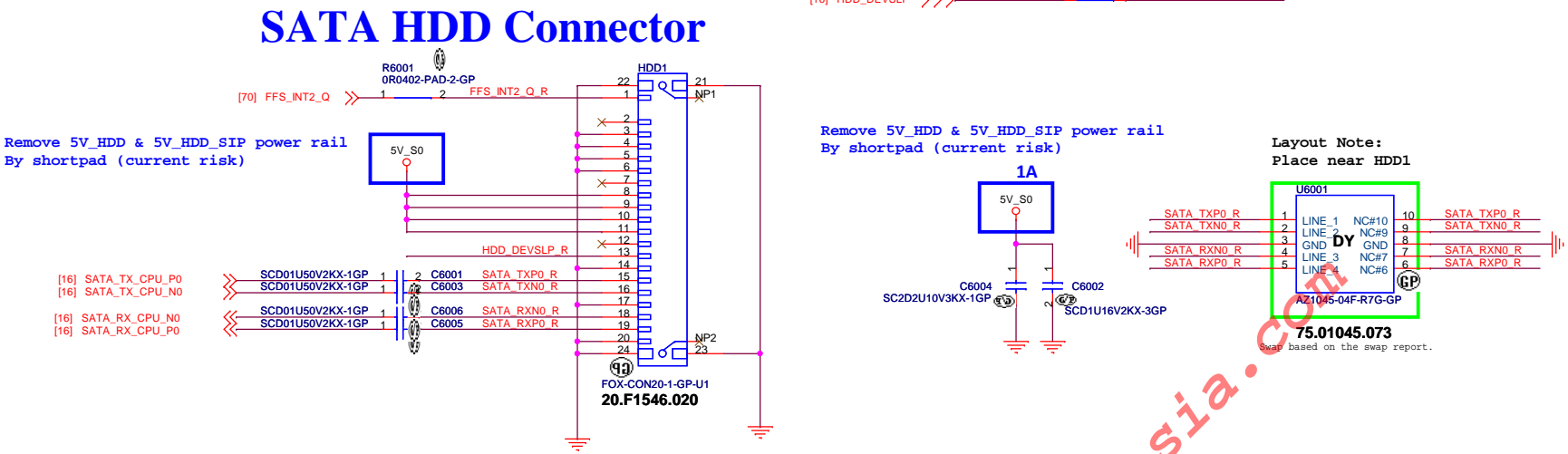
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Main Func = HDD




CONN		FFC
GND	S1	1
A+	S2	2
A-	S3	3
GND	S4	4
B-	S5	5
B+	S6	6
GND	S7	7
GND	P1	
GND	P2	
GND	P3	
5V	P4	10
5V	P5	11
5V	P6	12
GND	P7	
GND	P8	

Main Func = ODD

Main Func = WLAN

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NGFF WLAN CONN


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Main Func = Power BTN

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Title

LED Board&Power Button

Size
A3

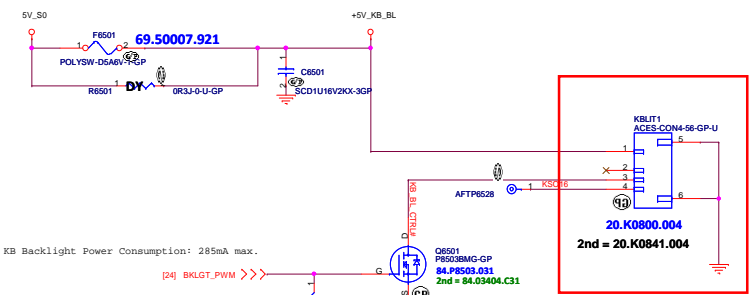
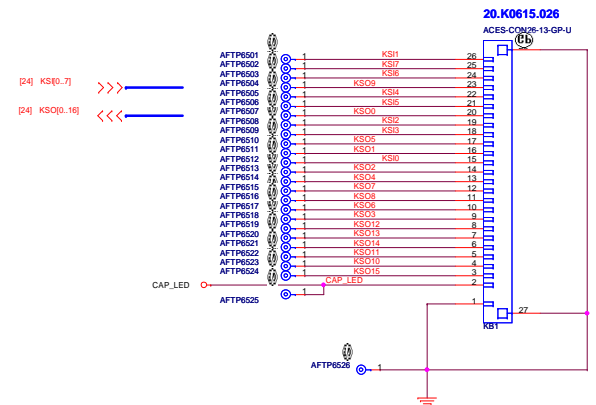
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Keyboard



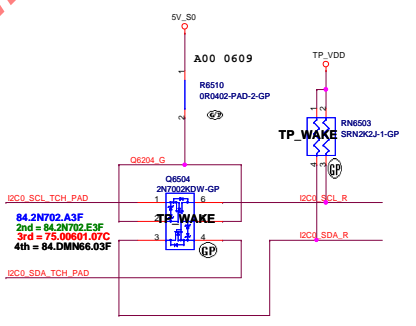
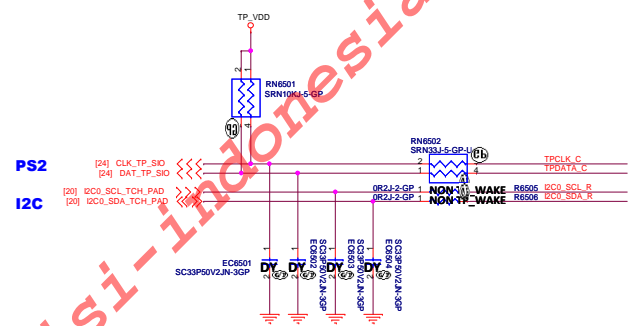
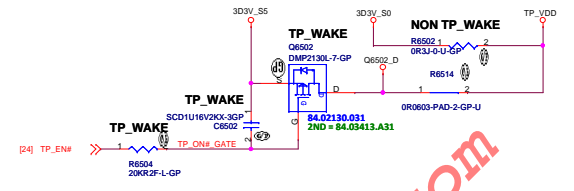
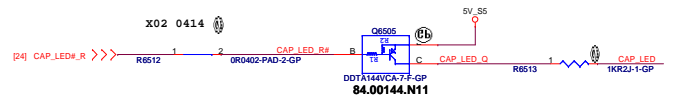
KB Backlight Power Consumption: 285mA max.

[24] BKLG_T_PWM >>>

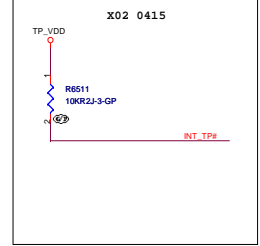
[24] BKL_CTL# >>>

Modify at DVT1 20150127
Change component by Lock function

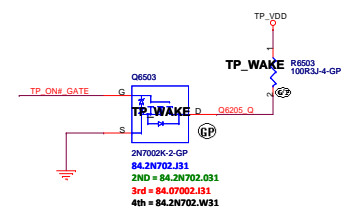
CAP LED Control
LOW actived from KBC GPIO



Need to check if it is Active High or Active Low and check if there is PH on TPAD side.

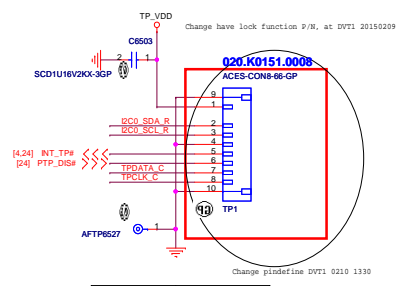


TP_VDD Discharge Circuit

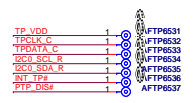


GPIO_TPAD: TBD
(Touch pad wake# for S3 wake up @ PCH GPIO??)

Touch Pad Connector

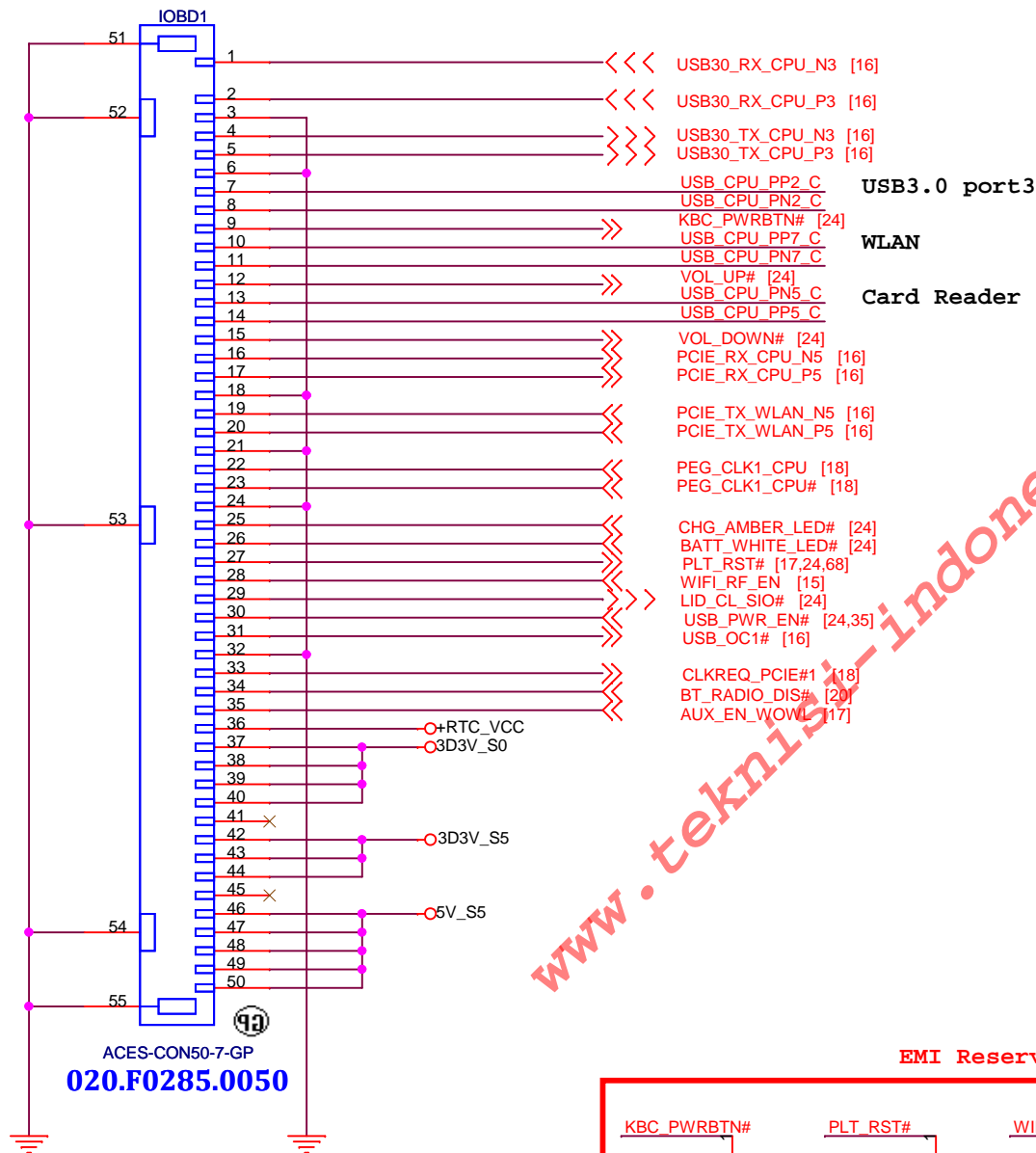


Pin number	Pin name
1	VDD
2	DAT (I2C)
3	CLK (I2C)
4	GND
5	ATTN
6	GPIO
7	DAT (PS2)
8	CLK (PS2)



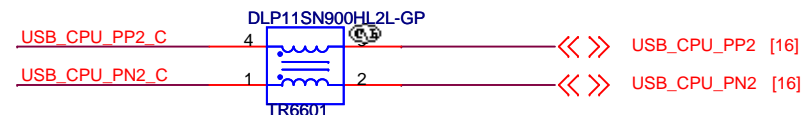
<Core Design>

Main Func = IO Connector

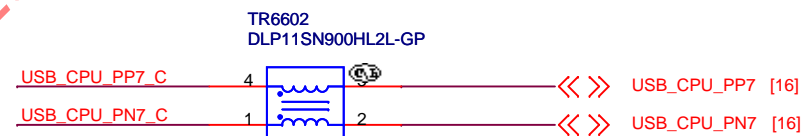


Power Pin Count : 10
GND Pin Count : 5

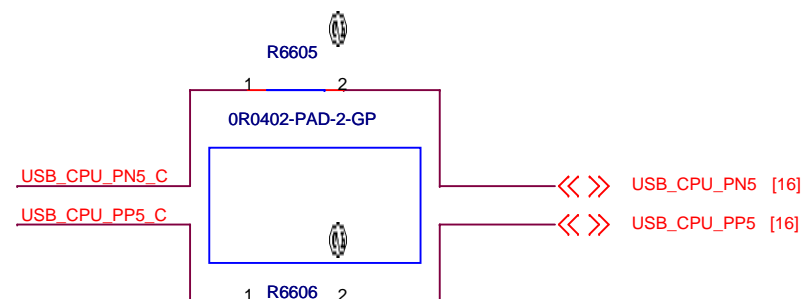
EMI Reserve , 20141118



Remove 00hm pad R6601,R6602 by A00 version

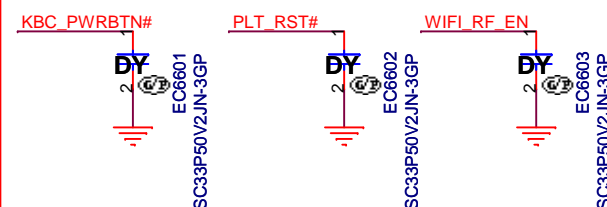


Remove 00hm pad R6603,R6604 by A00 version



Remove CMC TR6603 by A00 version

EMI Reserve , 20141118



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Title

IO Board Connector

Size
A4

Document Number

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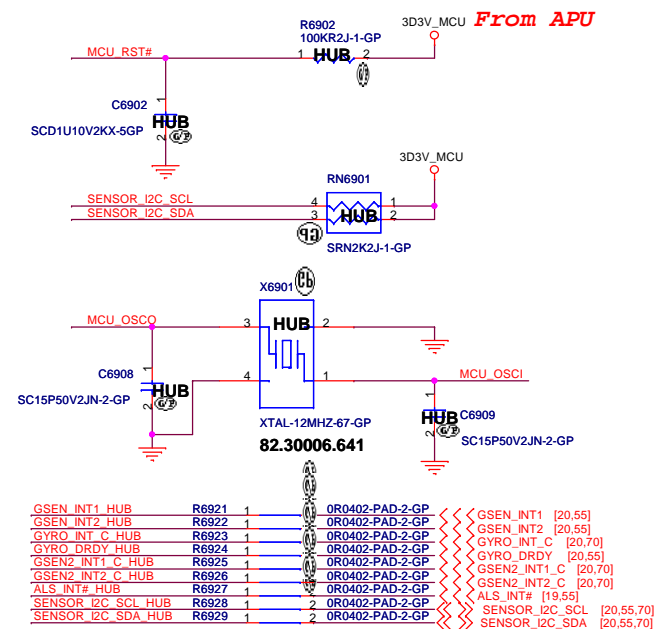
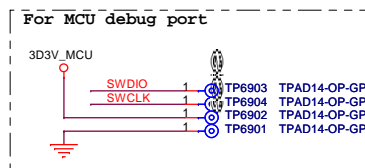
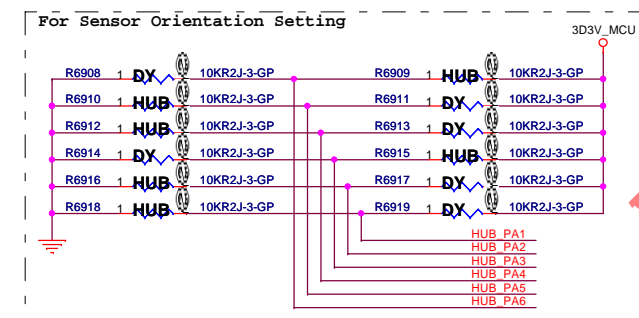
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USB3.0 PORT


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Main Func = dGPU

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GPU(55)PWR/GND

Size

Document Number

Rev

Custom

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A00

Date


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Main Func = dGPU

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GPU-VRAM1,2 (1/4)

Size
A3

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Main Func = dGPU

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GPU-VRAM3,4 (2/4)

Size
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Main Func = dGPU

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Main Func = dGPU

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Title

GPU-VRAM7,8 (4/4)

Size
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Main Func = dGFX_CORE
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GPU CORE


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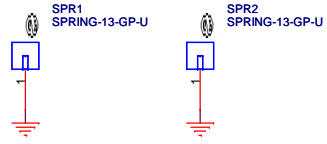
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Reserved

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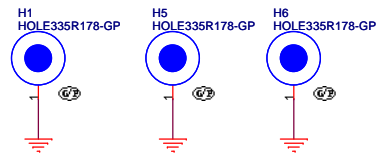
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34.43E24.001

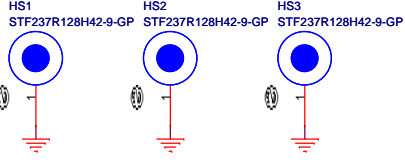


DVT1 0212 for ME

ZZ.00PAD.7F1

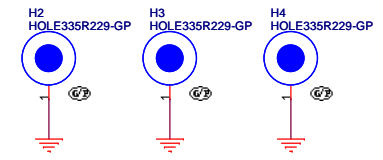


34.4WZ01.201



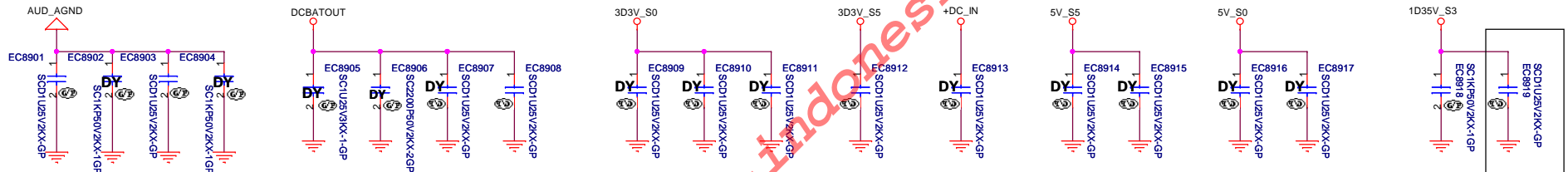
Modify at DVT1 20150204

ZZ.00PAD.7G1



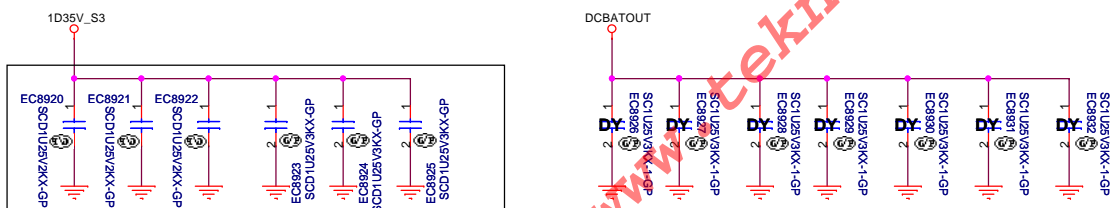
SSID = EMI

Mind the voltage rating of the caps.

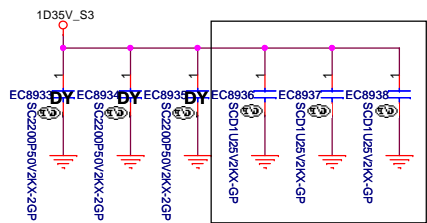


Change to 0.1uF at 20150427 for EMI

SSID = RF



Change to 0.1uF at 20150427 for EMI




Change to 0.1uF at 20150427 for EMI

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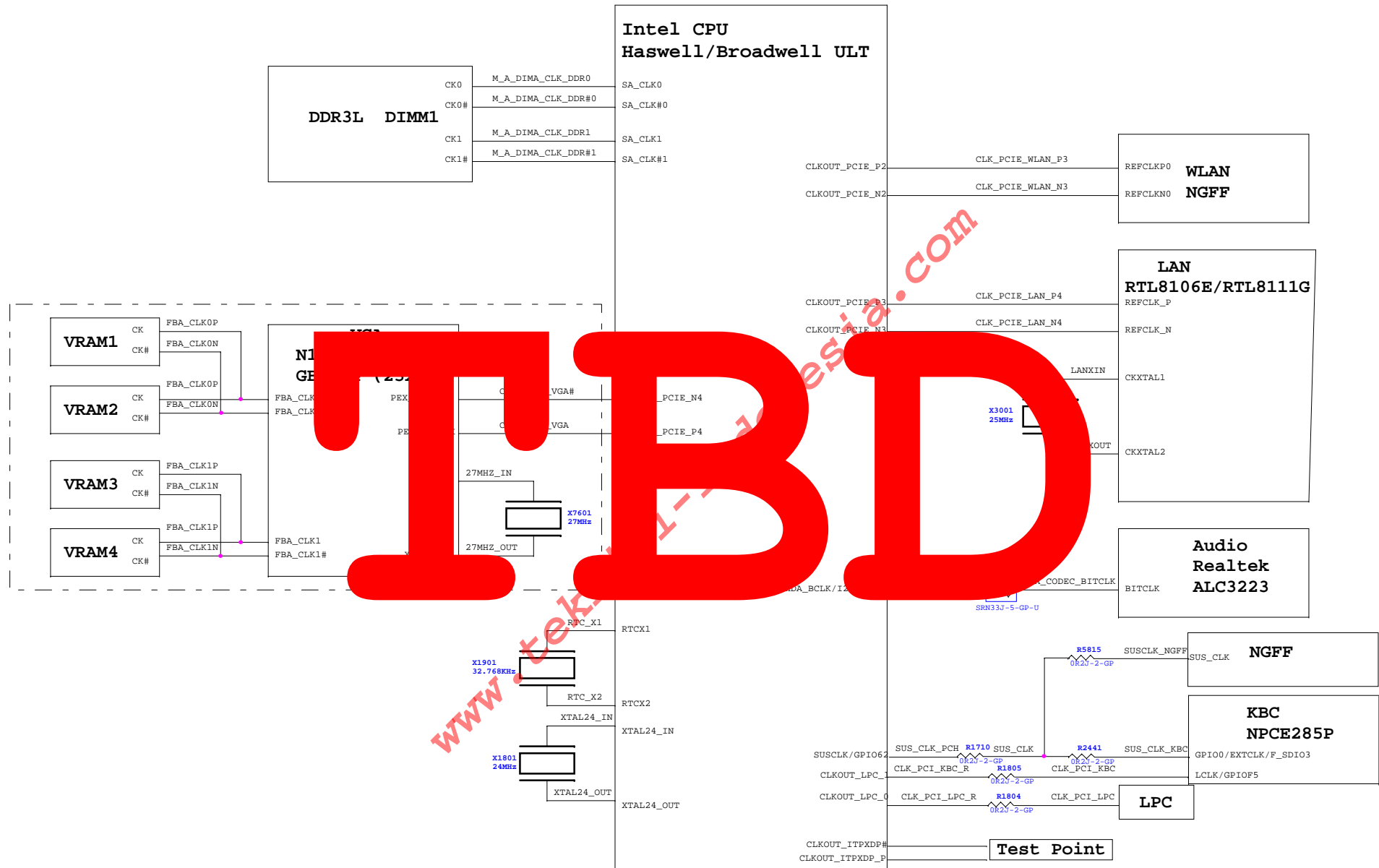
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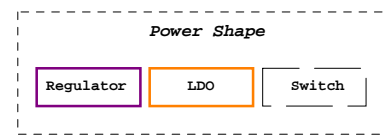
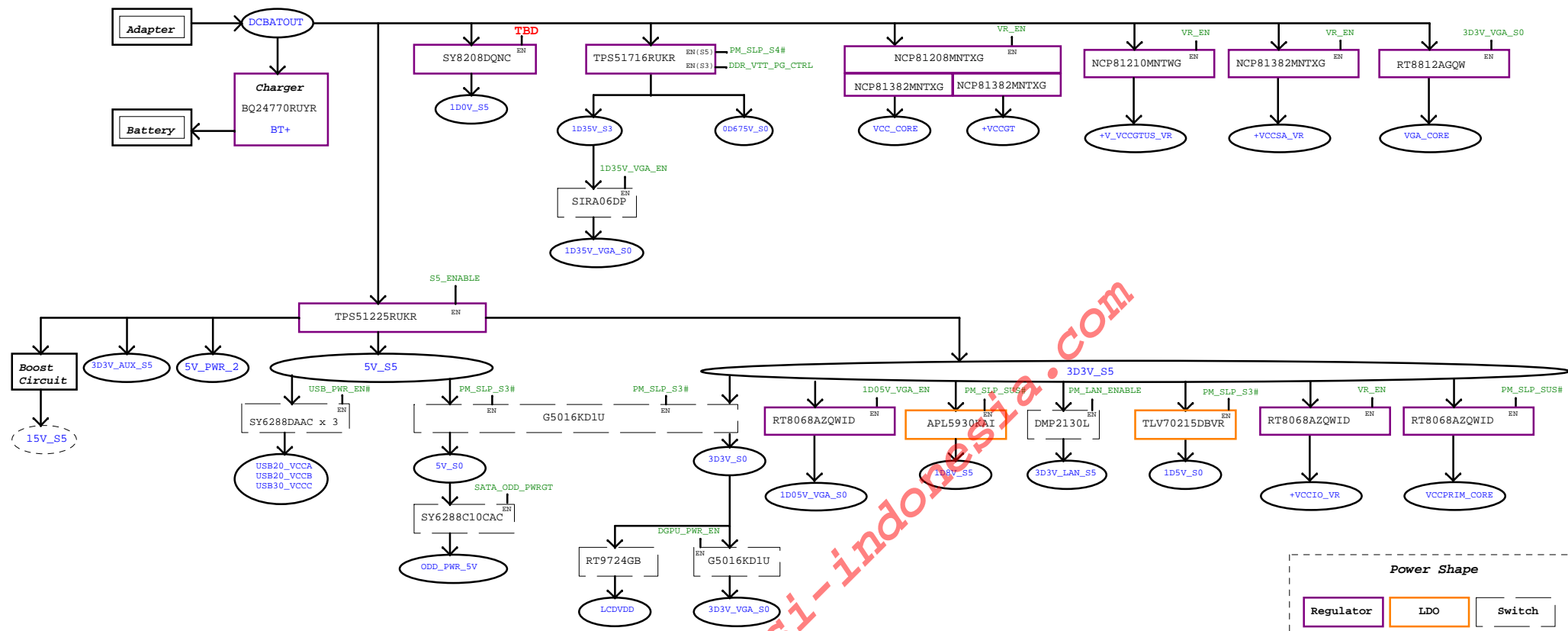
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Size	Document Number				Rev
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CLK Block Diagram



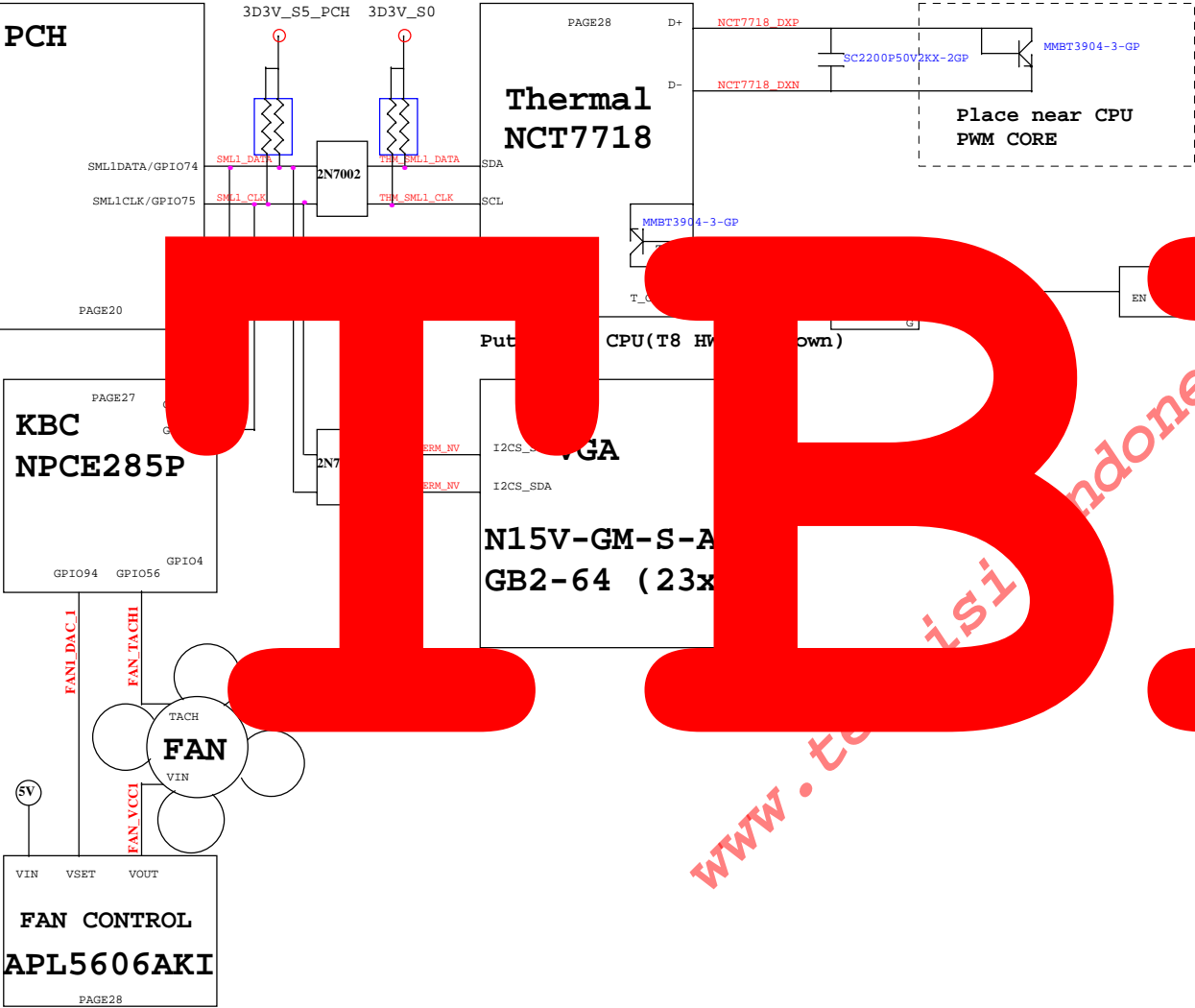
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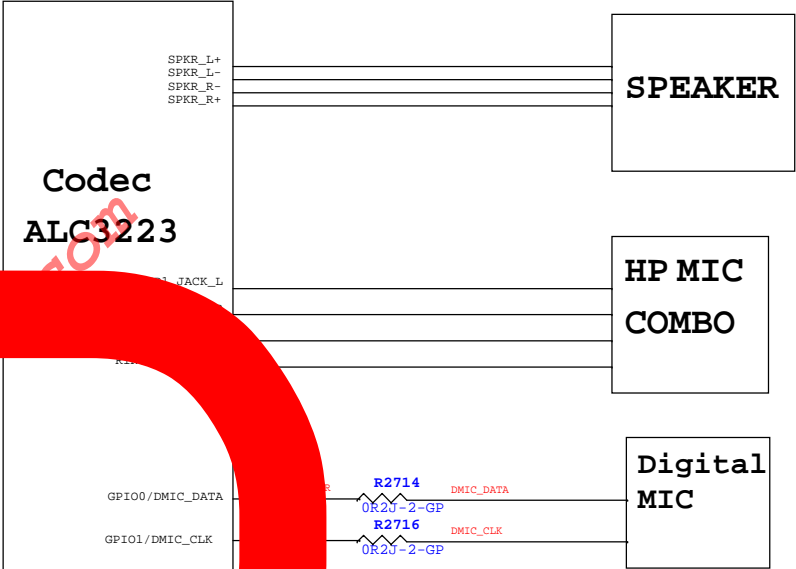


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Thermal Block Diagram



Audio Block Diagram



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